高速訊號基頻模組

P/N: **ZYNQ_TELV3.1**

ZYNQ_TEL V3.1 is designed for communication equipment as signal processing and control application. This module builds with Xilinx Zynq-7000 series SOC chip and high speed ADC & DAC which has excellent wideband and narrowband spurious-free dynamic range. It futures precise clock generation, adjustable I/O voltage, watchdog timer, 2 channels of 250MSPS analog input and output.

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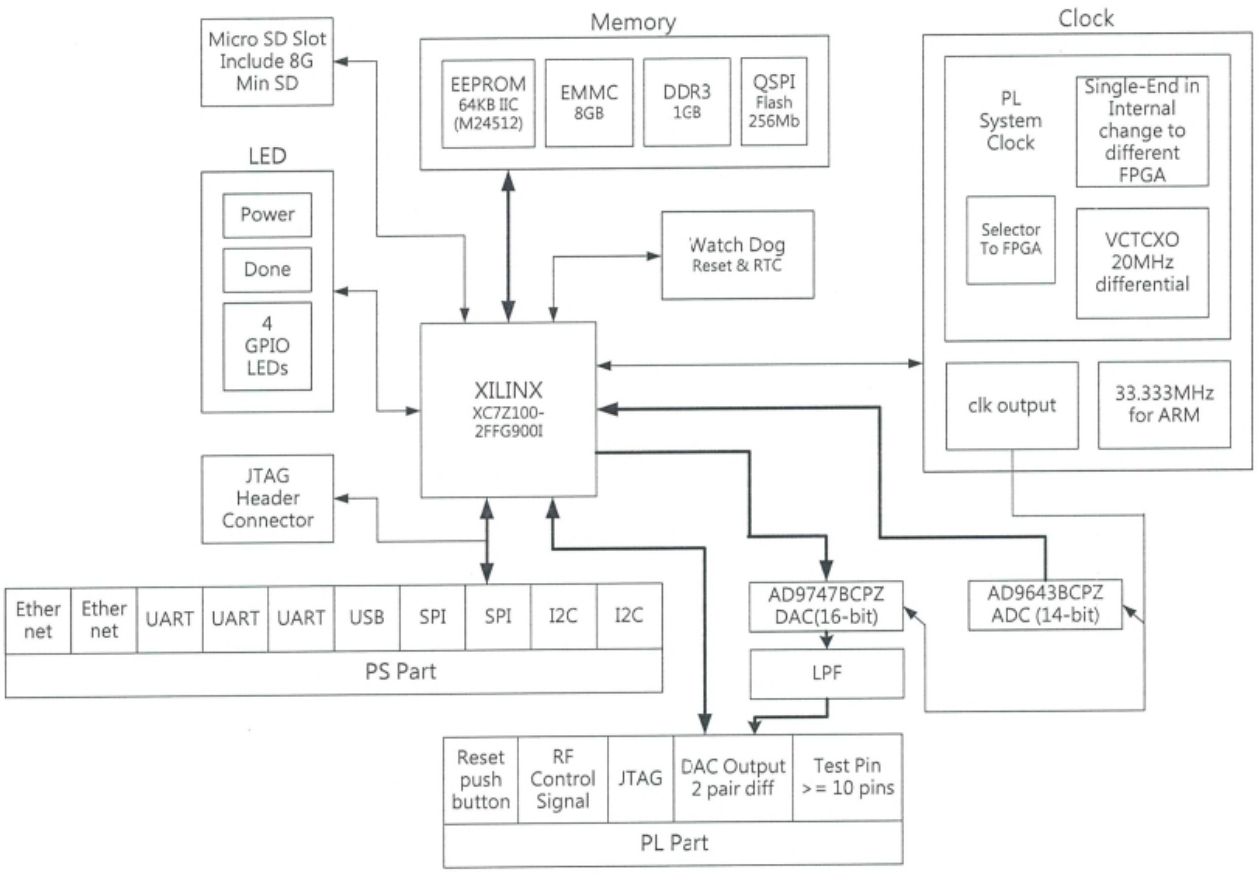
Specifications

· Xilinx XC7Z100-2FFG900I FPGA Main Processor
· 33.333MHz ±1%of PS System Clock Rate
· VCTXO 20MHzProgrammable Reference Clock
· FPGA External Reference Clock / Local Clock Input Switchable
· 1GB DDR3 Component Memory for PS
· 8GB EMMC Memory
· Micro SD Slot with 8GB Card * 1
· 256MbitQSPI Flash Memory* 1
· Analog Device AD9747BCPZ16-bit250MSPS DAC * 1
· Analog Device AD9643BCPZ-25014-bit 250MSPS ADC *1with ≦-92dBm Noise Level
· ADC and DAC Reference Clock Input Direct From FPGA
· Male SSMB Connector for ADC Signal Input
· 3 Bank of Adjust Voltage(1.8/2.5/3.3V) I/O Pins, default is 3.3V
· 64KByesof EEPROM Memory
· Programmable Watch Dog Timer, 1sec Default with External Power to RTC
· FPGA JTAG Port * 1
· UART Interface Port * 3
· Ethernet (10/100) Interface (I/O Connector) * 2
· USB2.0 Interface (I/O Connector) * 1
· SMD 0603 LED Indicator* 6(Power x 1, GPIO x 4, FPGA Done x 1)
· Male SSMB External Reference Clock Input* 1
· System Reset from I/O Connector * 1
· Single +5V±0.5V DC Power Input
· Total 152Pin User I/O Connector
· 181(W)x 67.6(D)mm+/-2mm Board Size

FPGA Block Diagram



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