RTL8305SC

SINGLE-CHIP 5-PORT 10/100MBPS SWITCH CONTROLLER WITH DUAL MII INTERFACES

RMII Application Note

Rev. 1.0
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Realtek Semiconductor Corp.
No. 2, Industry E. Rd. IX, Science-Based Industrial Park, Hsinchu 300, Taiwan
Tel: +886-3-5780211 Fax: +886-3-5776047
www.realtek.com.tw

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8305SC controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
Pre-1.0	2005/04/12	First release.

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1. General Description

The RTL8305SC is a 5-port Fast Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. The RTL8305SC also provide one RMII interface (port0) + four UTP ports (port 1~4) for system application.

2. Pin Assignments

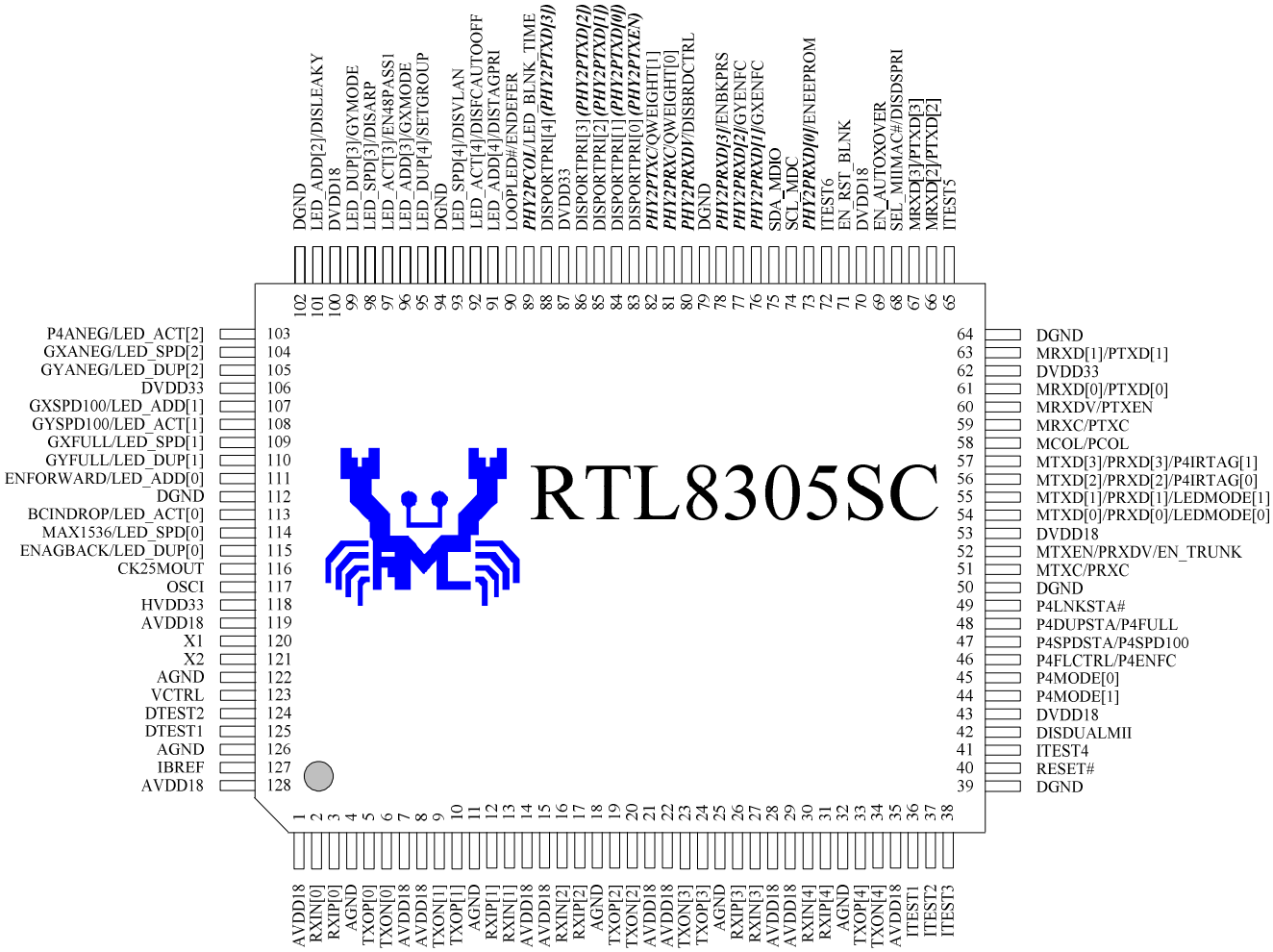

Figure 1. RTL8305SC Pin Assignments

3. System Application and Hardware Setting

3.1. External circuit block diagram for RTL8305SC RMII application

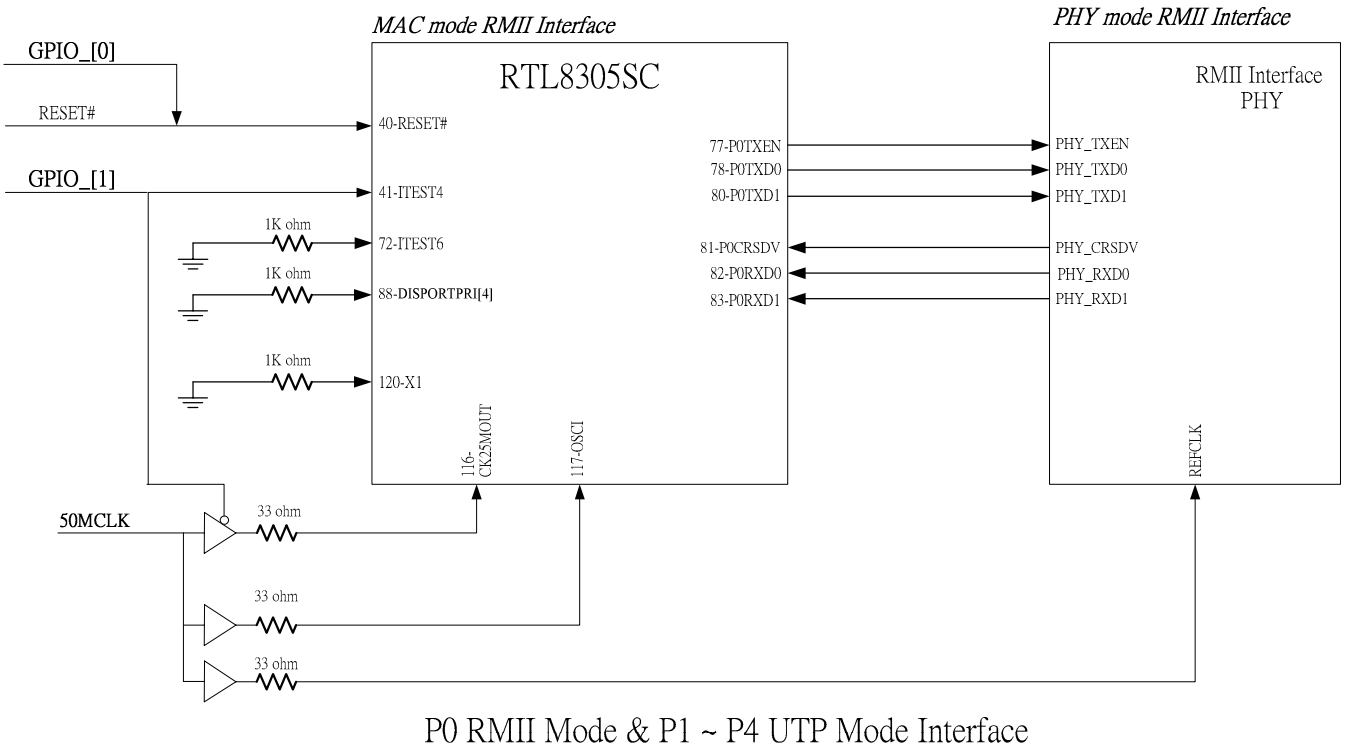

Figure 2. RTL8305SC RMII Application circuit Block Diagram

3.2. Hardware setting

When using RTL8305SC as Port0 RMII and Port1~4 UTP mode interface, please check the hardware pin setting as below:

Table 1. Strapping Pins

Pin Name	Pin No.	Type	Description
ITEST6	72		Must use 1k resistor to pull down to ground.
DISPORTPRI[4]	88		Must use 1k resistor to pull down to ground.

Pin Name	Pin No.	Type	Description
X1	120		Must use 1k resistor to pull down to ground.
OSCI	117	I	A 50MHz clock input from oscillator is fed to this pin. The X1 should be tied to ground and X2 should be left floating in this application.
RESET#	40	I	Active low reset signal. To complete the reset function, this pin must be asserted for at least 1ms. After reset, about 30ms is needed for the RTL8305SC to complete internal test functions and initialization. This pin is a Schmitt input. ***Need controlled by GPIO in this application. (note1)***
ITEST4	41		***Need controlled by GPIO in this application. (note1)***
CK25MOUT	116	O	A 50MHz clock input from oscillator is fed to this pin. ***Need controlled by GPIO in this application. (note1)***

Note1: GPIO[1:0] and CK25MOUT timing sequence shows as Figure 3. and Table 2.

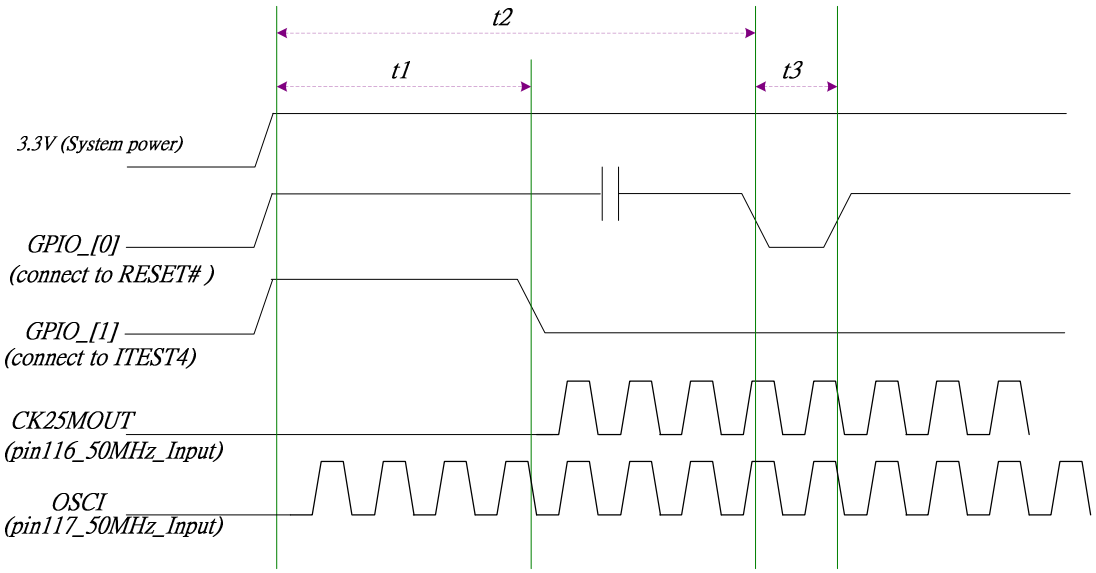

Figure 3. GPIO[1:0] and System Clock (50MHz) Timing Sequence

Table 2. GPIO[1:0] and System Clock (50MHz) Timing Sequence

Symbol	Description	Minimum	Typical	Maximum	Units
t1	Initiate GPIO[1] =1, delay t1, set GPIO[1]=0	100			ms
t2	Initiate GPIO[0] =1, delay t2, set GPIO[0]=0	200			ms
t3	Delay t3, set GPIO[0] = 1	50			ms

3.3. Port 0 RMII Interface Pins

When using RTL8305SC as Port0 RMII and Port1~4 UTP mode interface, the port 0 RMII interface pins show as below:

Table 3. Port 0 RMII Interface Pins

Pin Name	Pin No.	Type	Description
P0TXD[1:0]	80,78	O	**Port 0 RMII Transmit Data [1:0]** The RTL8305SC transmit data TXD[1:0] are clocked out by the rising edge of CK25MOUT(50MHz).
P0RXD[1:0]	83,82	I	**Port 0 RMII Receive Data [1:0]** The RTL8305SC sample the receive data RXD[1:0] on the rising edge of REFCLK when CRSDV is high.
P0TXEN	77	O	**RMII Transmit Enable** The RTL8305SC asserts high to indicate that valid data for transmission is presented on the P0TXD[1:0]. It is synchronous to CK25MOUT(50MHz).
P0CRSDV	81	I	**RMII CRSDV signals** CRSDV from PHY device is asserted high when media is non-idle.

3.4. Port 1~ 4 Media Connection Pins

When using RTL8305SC as Port0 RMII and Port1~4 UTP mode interface, the port 1~4 media(UTP) interface pins show as below:

Table 4. Port 1~4 Media Connection Pins

Pin Name	Pin No.	Type	Description
RXIP[4:1] RXIN[4:1]	12, 13, 16, 17, 26, 27, 30, 31	I	Differential Receive Data Input. Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].
TXOP[4:1] TXON[4:1]	9, 10, 19, 20, 23, 24, 33, 34	O	Differential Transmit Data Output. Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].

Because Port 0 is using RMII interface to connect with other device, therefore, that is recommend pull down Port 0 TXOP/N, RXIP/N signals to ground via 1k resistor.

Table 5. Port 0 Media Connection Pins

Pin Name	Pin No.	Type	Description
RXIP[0] RXIN[0]	3 2	I	Port 0 Differential Receive Data Input. Recommend using 1k resistor to pull down to ground.
TXOP[0] TXON[0]	5 6	O	Port 0 Differential Transmit Data Output. Recommend using 1k resistor to pull down to ground.

3.5. Miscellaneous Pins

Table 6. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
X1	120	I	A 25MHz crystal input. The clock tolerance is +-50ppm. When using an oscillator, this pin should be tied to ground.
X2	121	O	For crystal input. When using an oscillator, this pin should be left floating.
IBREF	127	A	Control transmit output waveform Vpp. This pin should be grounded through a 1.96KΩ resistor.
VCTRL	123	O	Voltage control to external regulator. This signal controls a power PNP transistor to generate the 1.8V power supply.
ITEST1	36		Reserved pin for internal use. Should be left floating.
ITEST2	37		Reserved pin for internal use. Should be left floating.
ITEST3	38		Reserved pin for internal use. Should be left floating.
ITEST5	65		Reserved pin for internal use. Should be left floating.
DTEST2	124		Reserved pin for internal use. Should be left floating.
DTEST1	125		Reserved pin for internal use. Should be left floating.

4. Port 0 RMII Timing Chart

4.1. Port 0 RMII Transmit Timing

Table 7. P0 RMII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_txd_rmii	REFCLK rising edge to TXD/TX_EN delay.	5		14.5	ns

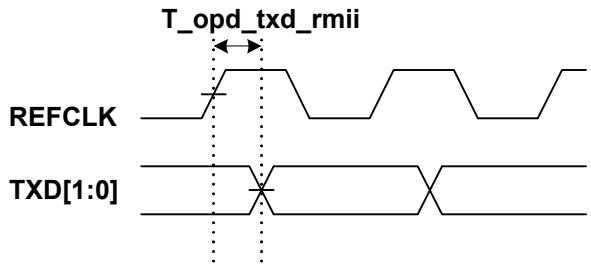

Figure 4. P0 RMII Transmit Timing

4.2. P0 RMII Receive Timing Request

Table 8. P0 RMII Transmit Timing Request

Symbol	Description	Minimum	Typical	Maximum	Units
T_ipsu_rxd_rmii	RXD/CRS_DV setup time to REFCLK.	4			ns
T_iphd_rxd_rmii	RXD/CRS_DV hold time from REFCLK.	2			ns

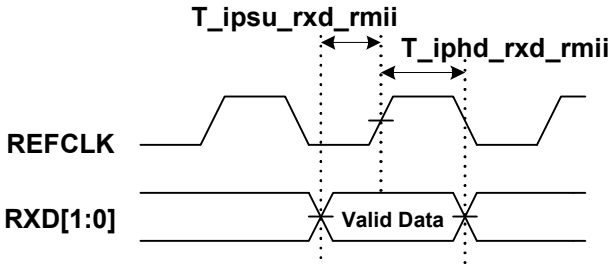

Figure 5. P0 RMII Receive Timing Request

Realtek Semiconductor Corp.
Headquarters
No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com.tw