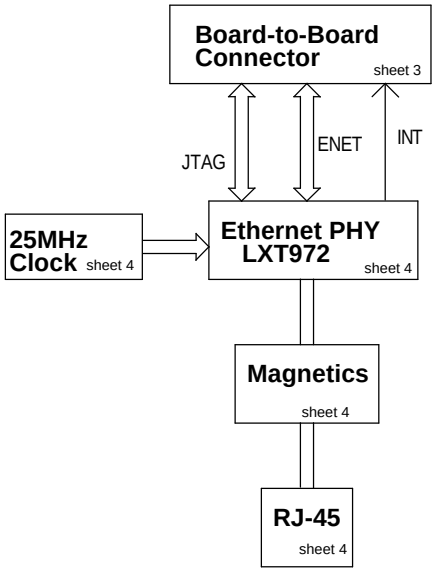
ETHERNET PHY CARD

for BIXMB425AD Network Processor Base Card



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2200 Mission College Blvd
Santa Clara, CA 95052

Title	**BIXD100 ETHERNET PHY CARD**	
Size B	Page Title: Title Page / Block Diagram	Rev 0.97
Date: Wednesday, July 10, 2002	Sheet 1 of 4	

SCHEMATIC ANNOTATIONS

VOLTAGE RAILS

+12V	Not used on this module. Generated on IXP425 baseboard.
+5V	Not used on this module. Generated on IXP425 baseboard.
+3V3	Generated on IXP425 baseboard. Supplied to the LXT972 and surrounding circuitry.
+3V3_ENET	Analog power generated from +3.3V on this module. Supplied to the LXT972 and surrounding circuitry.
+2.5V	Not used on this module. Generated on IXP425 baseboard.
-32V	Not used on this module. Generated on IXP425 baseboard.
-64V	Not used on this module. Generated on IXP425 baseboard.

GROUNDS

GND_DIGITAL	Digital Ground Plane

DESIGN NOTES

0.0 ohm resistors are placed to allow accessiblity to nodes that may be of interest.

_DNP	Do Not Populate this component if this designation is found on component's schematic.

REVISION HISTORY

Rev 0.97 * Schematics for prototype build

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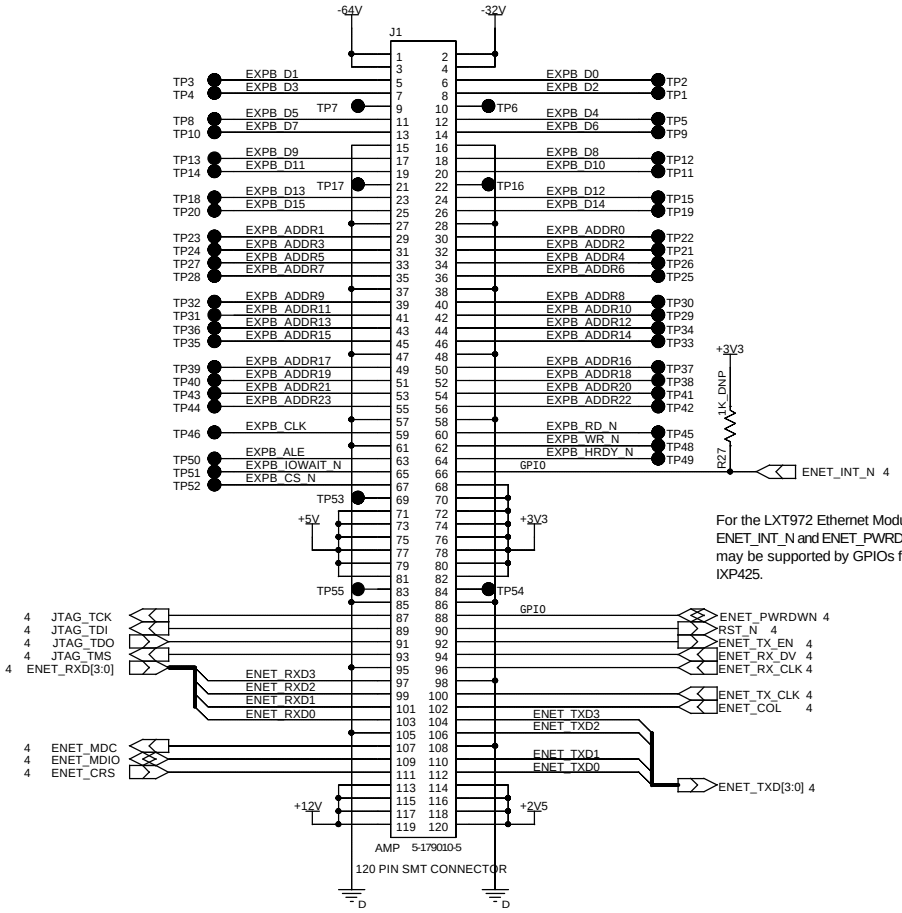
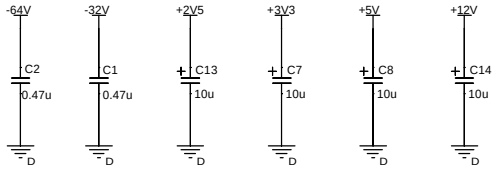
Title	BIXD100 ETHERNET PHY CARD	
Size B	Page Title: Schematic Notes	Rev 0.97
Date: Wednesday, July 10, 2002	Sheet 2 of 4	



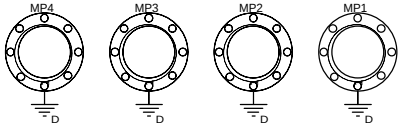
For the LXT972 Ethernet Module, ENET_INT_N and ENET_PWRDWN may be supported by GPIOs from the IXP425.



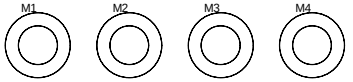
Note: One 250V 0.47uF decoupling capacitor is used for the -32V and -64V voltage rails

Note: One 10uF decoupling capacitor is used for each positive voltage power pin.

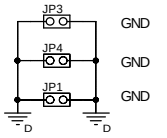
MP1-MP4 are to be placed in the four corners of the board.



M1-M4 are to be placed along the board edge.



Silkscreen:



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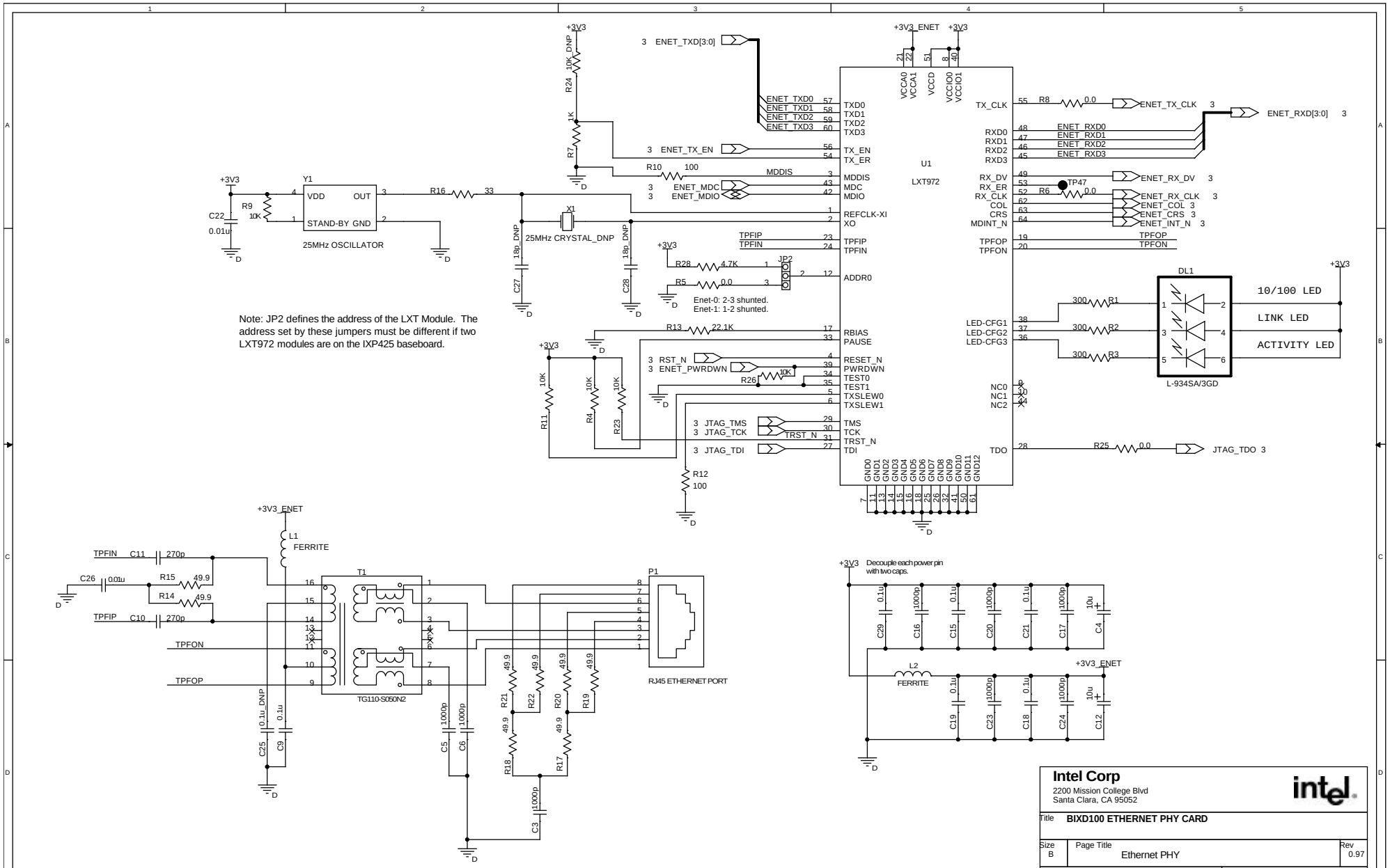
Size	Page Title	Rev
B	Board-To-Board Connector	0.97

Date: Wednesday, July 10, 2002 Sheet 3 of 4


Note: JP2 defines the address of the LXT Module. The address set by these jumpers must be different if two LXT972 modules are on the IXP425 baseboard.
25MHz OSCILLATOR
25MHz CRYSTAL_DNP
Enet-0: 2-3 shunted.
Enet-1: 1-2 shunted.
U1
LXT972
L-934SA/3GD
10/100 LED
LINK LED
ACTIVITY LED
TG110-S050N2
RJ45 ETHERNET PORT
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BIXD100 ETHERNET PHY CARD
Ethernet PHY
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