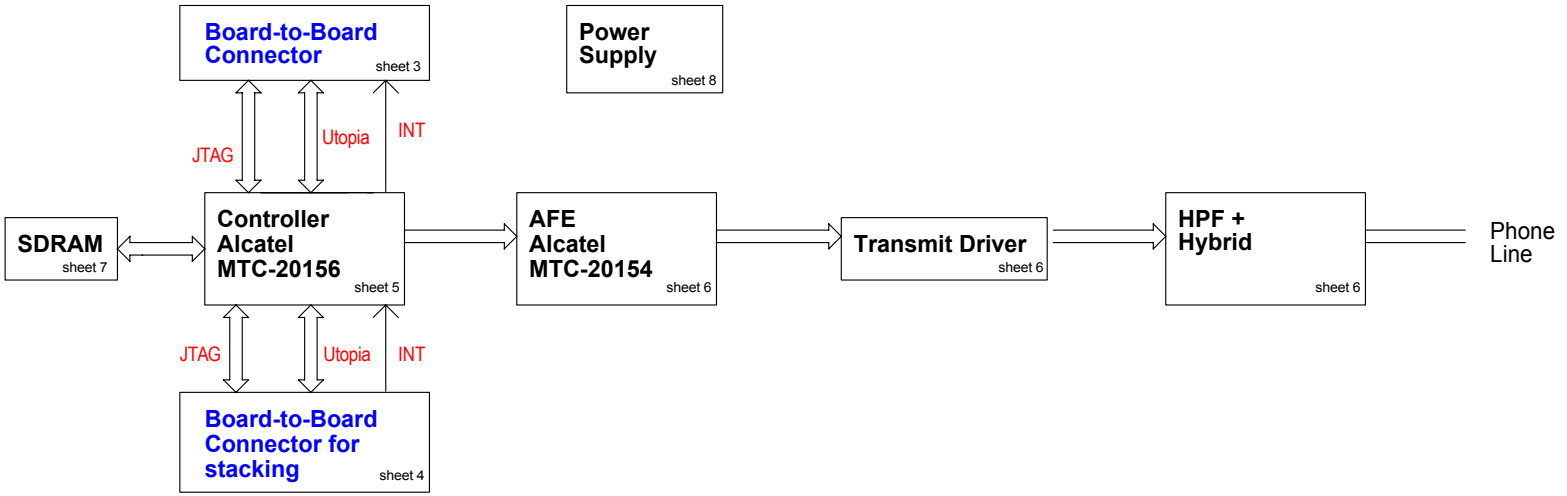
ADSL ANNEX A PHY CARD

for BIXMB425AD Network Processor Base Card



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SCHEMATIC ANNOTATIONS

VOLTAGE RAILS

+12VIN	Provided from IXP425 baseboard.
+12V	Generated on module.
CPE_DRV_12VPOS	Derived from the +12V rail.
CO_DRV_12VPOS	Derived from the +12V rail.
+5V	Not used on this module. Provided from IXP425 baseboard.
+3V3	Provided by IXP425 baseboard.
20156_3V3	Derived from the +3V3 rail.
20154_A23V3	Derived from the +3V3 rail.
20154_D3V3	Derived from the +3V3 rail.
+2V5	Provided from IXP425 baseboard.
20156_2V5	Derived from the +2V5 rail.
-12V	Derived from the +3V3 rail.
CPE_DRV_12VNEG	Derived from the -12V rail.
CO_DRV_12VNEG	Derived from the -12V rail.

GROUNDS

GND_DIGITAL	Digital Ground Plane (designated by "D" on ground symbol)
GND_ANALOG	Analog Ground Plane (designated by "A" on ground symbol)
GND_POWERSUPPLY	Power Supply Ground Plane (designated by "PSGND" near ground symbol)
SHIELD	Shield ground.

DESIGN NOTES

0.0 ohm resistors are placed to allow accessiblity to nodes that may be of interest.

_DNP	Do Not Populate this component if this designation is found on component's schematic.

REVISION HISTORY

Rev 0.95 * Schematics for prototype build.

Rev 0.99 * Updated with a NMOS transistor and a pull up resistor on IO_WAIT signal

Rev 0.99 * Updated with an 0 ohm resistor on IO_WAIT signal

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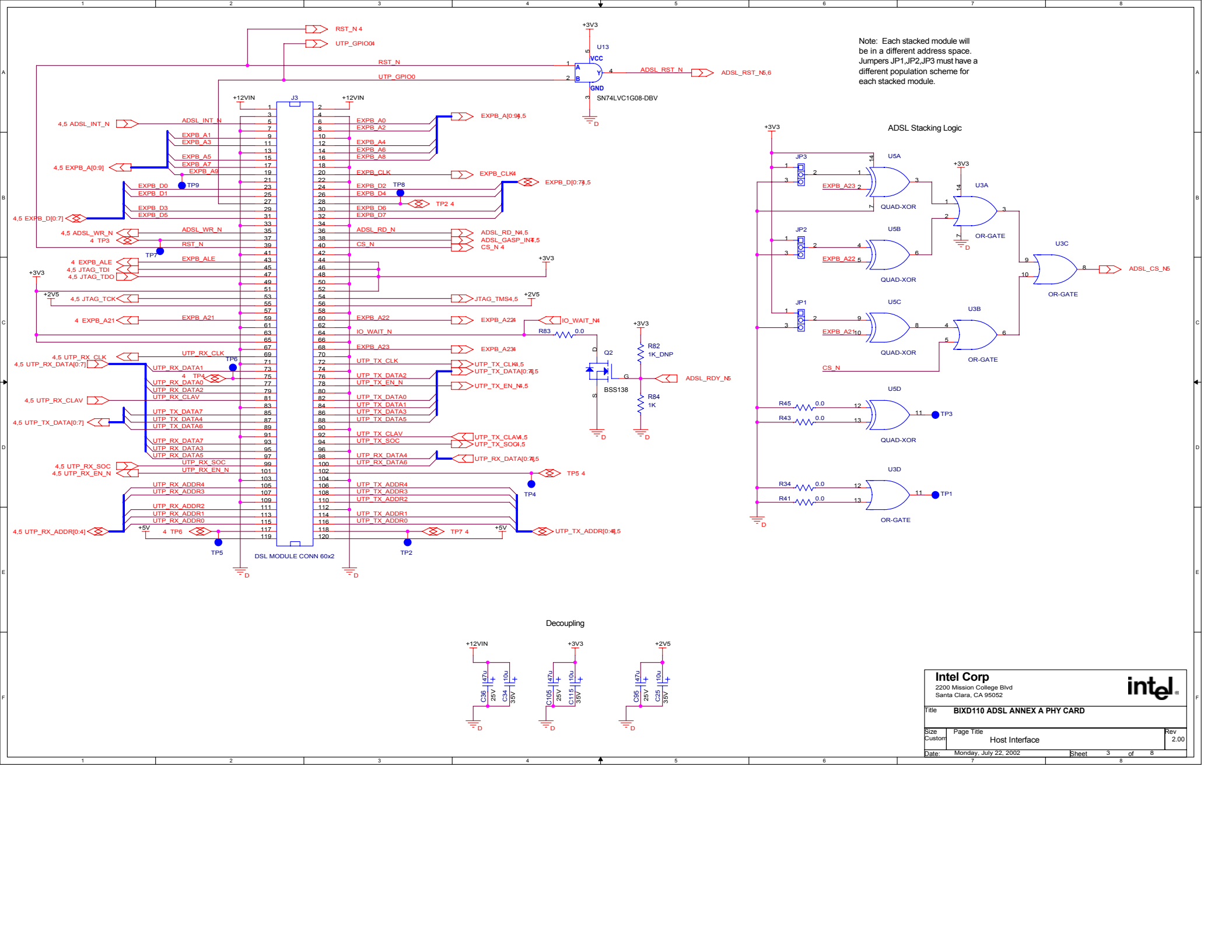
Note: Each stacked module will be in a different address space. Jumpers JP1,JP2,JP3 must have a different population scheme for each stacked module.
RST_N 4
UTP_GPIO0 4
RST_N
UTP_GPIO0
+3V3
U13
VCC
A
B
Y
GND
SN74LVC1G08-DBV
ADSL_RST_N
ADSL_RST_N5,6
+12VIN
J3
DSL MODULE CONN 60x2
4,5 ADSL_INT_N
ADSL_INT_N
4,5 EXPB_A[0:9]
EXPB_A[0:9]4,5
EXPB_A0
EXPB_A1
EXPB_A2
EXPB_A3
EXPB_A4
EXPB_A5
EXPB_A6
EXPB_A7
EXPB_A8
EXPB_A9
EXPB_CLK
EXPB_CLK4
EXPB_D0
EXPB_D1
EXPB_D2
EXPB_D3
EXPB_D4
EXPB_D5
EXPB_D6
EXPB_D7
EXPB_D[0:7]4,5
4,5 EXPB_D[0:7]
TP9
TP8
TP2 4
4,5 ADSL_WR_N
4 TP3
ADSL_WR_N
RST_N
TP7
ADSL_RD_N
ADSL_GASP_IN
CS_N 4
ADSL_RD_N4,5
ADSL_GASP_IN4,5
4 EXPB_ALE
4,5 JTAG_TDI
4,5 JTAG_TDO
EXPB_ALE
4,5 JTAG_TCK
JTAG_TMS4,5
4 EXPB_A21
EXPB_A21
EXPB_A22
EXPB_A22 4
IO_WAIT_N4
IO_WAIT_N
R83
0.0
EXPB_A23
EXPB_A23 4
4,5 UTP_RX_CLK
4,5 UTP_RX_DATA[0:7]
UTP_RX_CLK
TP6
UTP_RX_DATA1
4 TP4
UTP_RX_DATA0
UTP_RX_DATA2
UTP_RX_CLAV
4,5 UTP_RX_CLAV
4,5 UTP_TX_DATA[0:7]
UTP_TX_DATA7
UTP_TX_DATA4
UTP_TX_DATA6
UTP_RX_DATA7
UTP_RX_DATA3
UTP_RX_DATA5
UTP_RX_SOC
4,5 UTP_RX_SOC
4,5 UTP_RX_EN_N
UTP_RX_EN_N
UTP_TX_CLK
UTP_TX_EN_N
UTP_TX_CLK4,5
UTP_TX_DATA[0:7]4,5
UTP_TX_EN_N4,5
UTP_TX_DATA2
UTP_TX_DATA0
UTP_TX_DATA1
UTP_TX_DATA3
UTP_TX_DATA5
UTP_TX_CLAV
UTP_TX_SOC
UTP_TX_CLAV4,5
UTP_TX_SOC4,5
UTP_RX_DATA4
UTP_RX_DATA6
UTP_RX_DATA[0:7]4,5
TP5 4
TP4
Q2
BSS138
R82
1K_DNP
R84
1K
ADSL_RDY_N5
UTP_RX_ADDR4
UTP_RX_ADDR3
UTP_RX_ADDR2
UTP_RX_ADDR1
UTP_RX_ADDR0
4,5 UTP_RX_ADDR[0:4]
UTP_TX_ADDR4
UTP_TX_ADDR3
UTP_TX_ADDR2
UTP_TX_ADDR1
UTP_TX_ADDR0
UTP_TX_ADDR[0:4]4,5
+5V
4 TP6
TP7 4
TP5
TP2
ADSL Stacking Logic
JP3
JP2
JP1
U5A
U5B
U5C
U5D
U3A
U3B
U3C
U3D
QUAD-XOR
OR-GATE
EXPB_A23
EXPB_A22
EXPB_A21
CS_N
R45
R43
R34
R41
0.0
TP3
TP1
ADSL_CS_N5
Decoupling
C36
C34
C105
C115
C95
C25
47u
10u
25V
35V
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BIXD110 ADSL ANNEX A PHY CARD
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Host Interface
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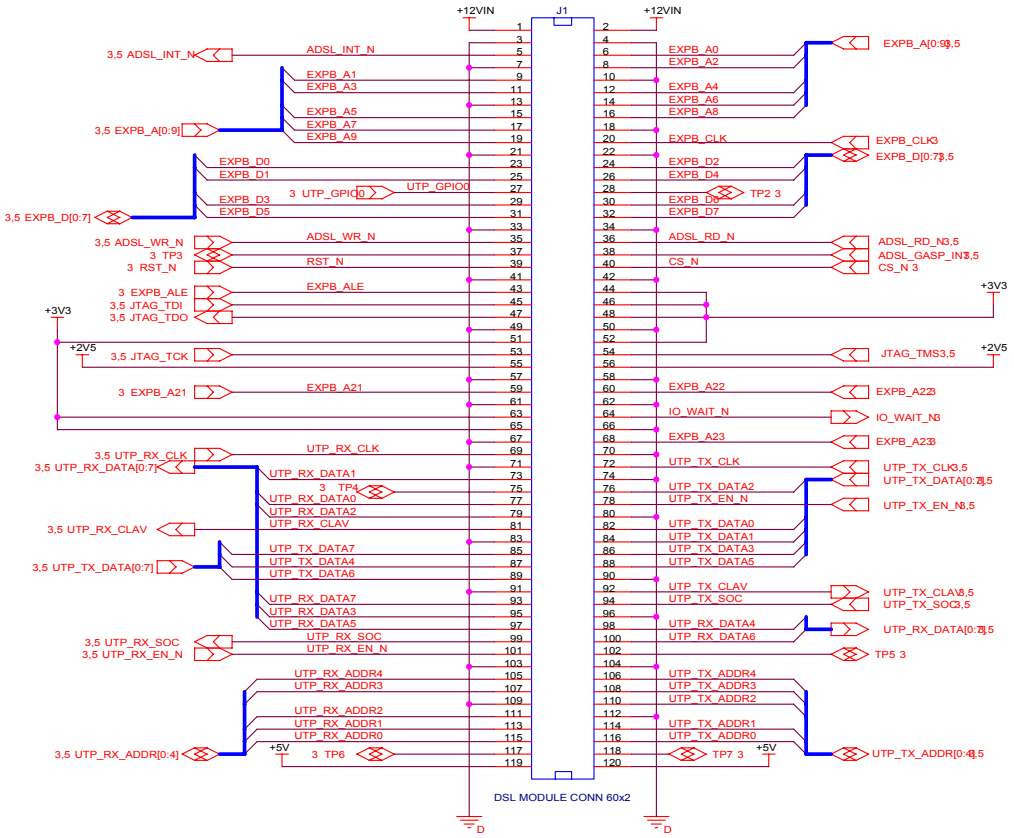

Note: This is the connector on the top side of the module. It is used to allow up to 4 Alcatel ADSL Modules to be stacked to enable multiple-channel use.

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Title	**BIXD110 ADSL ANNEX A PHY CARD**	
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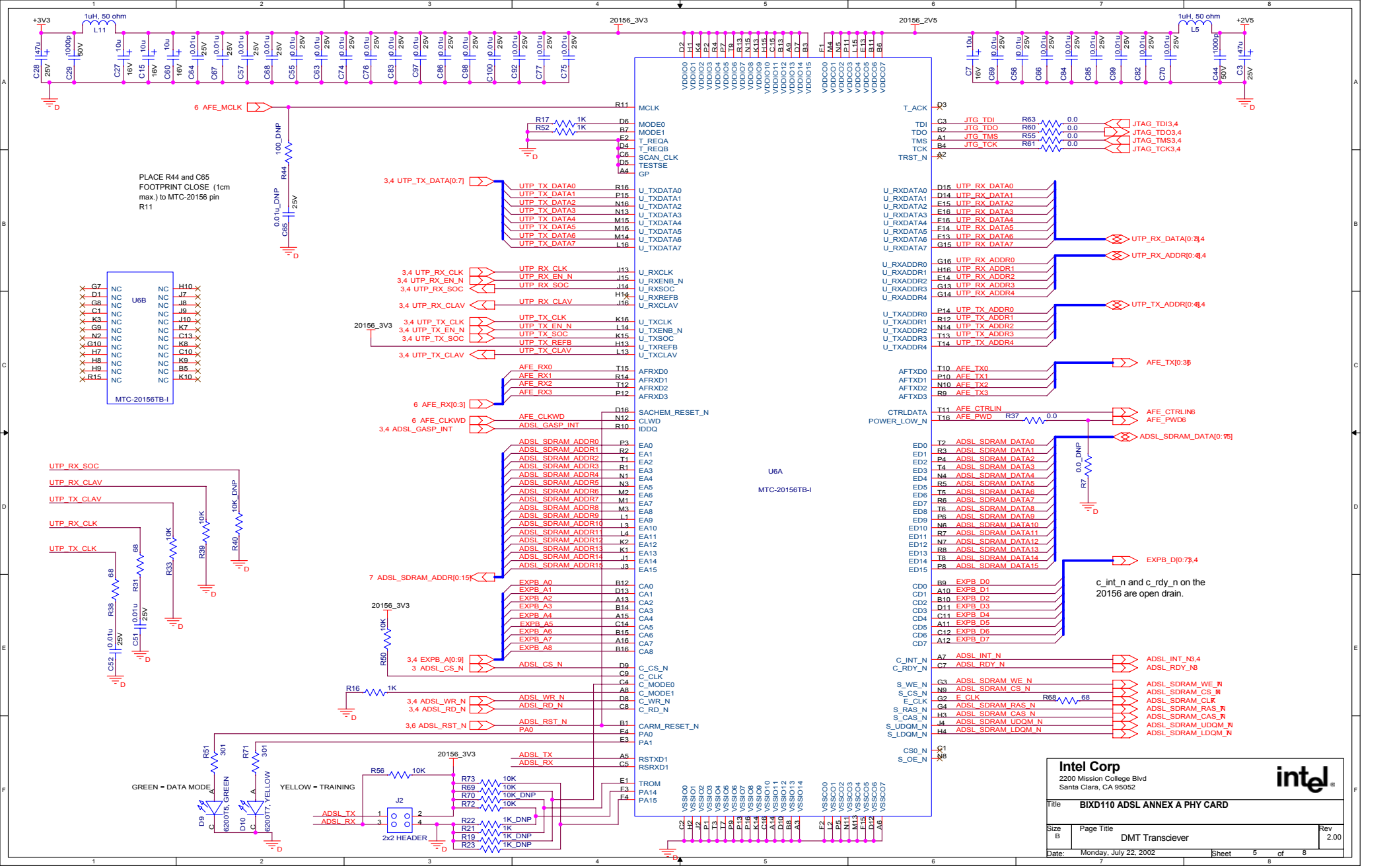
+3V3
1uH, 50 ohm
L11
20156_3V3
20156_2V5
+2V5
1uH, 50 ohm
L5
6 AFE_MCLK
R11
MCLK
T_ACK
D3
R17 1K
R52 1K
MODE0
MODE1
T_REQA
T_REQB
SCAN_CLK
TESTSE
GP
TDI
TDO
TMS
TCK
TRST_N
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
R63 0.0
R60 0.0
R55 0.0
R61 0.0
JTAG_TDI3,4
JTAG_TDO3,4
JTAG_TMS3,4
JTAG_TCK3,4
100_DNP
R44
0.01u_DNP
C65
25V
PLACE R44 and C65
FOOTPRINT CLOSE (1cm
max.) to MTC-20156 pin
R11
3,4 UTP_TX_DATA[0:7]
UTP_TX_DATA0
UTP_TX_DATA1
UTP_TX_DATA2
UTP_TX_DATA3
UTP_TX_DATA4
UTP_TX_DATA5
UTP_TX_DATA6
UTP_TX_DATA7
U_TXDATA0
U_TXDATA1
U_TXDATA2
U_TXDATA3
U_TXDATA4
U_TXDATA5
U_TXDATA6
U_TXDATA7
U_RXDATA0
U_RXDATA1
U_RXDATA2
U_RXDATA3
U_RXDATA4
U_RXDATA5
U_RXDATA6
U_RXDATA7
UTP_RX_DATA[0:7]
3,4
3,4 UTP_RX_CLK
3,4 UTP_RX_EN_N
3,4 UTP_RX_SOC
3,4 UTP_RX_CLAV
UTP_RX_CLK
UTP_RX_EN_N
UTP_RX_SOC
UTP_RX_CLAV
U_RXCLK
U_RXENB_N
U_RXSOC
U_RXREFB
U_RXCLAV
U_RXADDR0
U_RXADDR1
U_RXADDR2
U_RXADDR3
U_RXADDR4
UTP_RX_ADDR0
UTP_RX_ADDR1
UTP_RX_ADDR2
UTP_RX_ADDR3
UTP_RX_ADDR4
UTP_RX_ADDR[0:4]
3,4
20156_3V3
3,4 UTP_TX_CLK
3,4 UTP_TX_EN_N
3,4 UTP_TX_SOC
3,4 UTP_TX_CLAV
UTP_TX_CLK
UTP_TX_EN_N
UTP_TX_SOC
UTP_TX_REFB
UTP_TX_CLAV
U_TXCLK
U_TXENB_N
U_TXSOC
U_TXREFB
U_TXCLAV
U_TXADDR0
U_TXADDR1
U_TXADDR2
U_TXADDR3
U_TXADDR4
UTP_TX_ADDR0
UTP_TX_ADDR1
UTP_TX_ADDR2
UTP_TX_ADDR3
UTP_TX_ADDR4
UTP_TX_ADDR[0:4]
3,4
AFE_RX0
AFE_RX1
AFE_RX2
AFE_RX3
6 AFE_RX[0:3]
AFRXD0
AFRXD1
AFRXD2
AFRXD3
AFTXD0
AFTXD1
AFTXD2
AFTXD3
AFE_TX0
AFE_TX1
AFE_TX2
AFE_TX3
AFE_TX[0:3]
6
SACHEM_RESET_N
6 AFE_CLKWD
3,4 ADSL_GASP_INT
AFE_CLKWD
ADSL_GASP_INT
CLWD
IDDQ
CTRLDATA
POWER_LOW_N
AFE_CTRLIN
AFE_PWD
R37 0.0
AFE_CTRLIN6
AFE_PWD6
ADSL_SDRAM_DATA[0:15]
ADSL_SDRAM_ADDR0
ADSL_SDRAM_ADDR1
ADSL_SDRAM_ADDR2
ADSL_SDRAM_ADDR3
ADSL_SDRAM_ADDR4
ADSL_SDRAM_ADDR5
ADSL_SDRAM_ADDR6
ADSL_SDRAM_ADDR7
ADSL_SDRAM_ADDR8
ADSL_SDRAM_ADDR9
ADSL_SDRAM_ADDR10
ADSL_SDRAM_ADDR11
ADSL_SDRAM_ADDR12
ADSL_SDRAM_ADDR13
ADSL_SDRAM_ADDR14
ADSL_SDRAM_ADDR15
EA0
EA1
EA2
EA3
EA4
EA5
EA6
EA7
EA8
EA9
EA10
EA11
EA12
EA13
EA14
EA15
ED0
ED1
ED2
ED3
ED4
ED5
ED6
ED7
ED8
ED9
ED10
ED11
ED12
ED13
ED14
ED15
ADSL_SDRAM_DATA0
ADSL_SDRAM_DATA1
ADSL_SDRAM_DATA2
ADSL_SDRAM_DATA3
ADSL_SDRAM_DATA4
ADSL_SDRAM_DATA5
ADSL_SDRAM_DATA6
ADSL_SDRAM_DATA7
ADSL_SDRAM_DATA8
ADSL_SDRAM_DATA9
ADSL_SDRAM_DATA10
ADSL_SDRAM_DATA11
ADSL_SDRAM_DATA12
ADSL_SDRAM_DATA13
ADSL_SDRAM_DATA14
ADSL_SDRAM_DATA15
R7 0.0_DNP
7 ADSL_SDRAM_ADDR[0:15]
EXPB_D[0:7]
3,4
EXPB_A0
EXPB_A1
EXPB_A2
EXPB_A3
EXPB_A4
EXPB_A5
EXPB_A6
EXPB_A7
EXPB_A8
CA0
CA1
CA2
CA3
CA4
CA5
CA6
CA7
CA8
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
EXPB_D0
EXPB_D1
EXPB_D2
EXPB_D3
EXPB_D4
EXPB_D5
EXPB_D6
EXPB_D7
c_int_n and c_rdy_n on the
20156 are open drain.
20156_3V3
R50 10K
3,4 EXPB_A[0:9]
3 ADSL_CS_N
ADSL_CS_N
C_CS_N
C_CLK
C_MODE0
C_MODE1
C_WR_N
C_RD_N
C_INT_N
C_RDY_N
ADSL_INT_N
ADSL_RDY_N
ADSL_INT_N3,4
ADSL_RDY_N3
R16 1K
3,4 ADSL_WR_N
3,4 ADSL_RD_N
ADSL_WR_N
ADSL_RD_N
S_WE_N
S_CS_N
E_CLK
S_RAS_N
S_CAS_N
S_UDQM_N
S_LDQM_N
ADSL_SDRAM_WE_N
ADSL_SDRAM_CS_N
ADSL_SDRAM_CLK
ADSL_SDRAM_RAS_N
ADSL_SDRAM_CAS_N
ADSL_SDRAM_UDQM_N
ADSL_SDRAM_LDQM_N
R68 68
3,6 ADSL_RST_N
ADSL_RST_N
CARM_RESET_N
PA0
PA1
RSTXD1
RSRXD1
CS0_N
S_OE_N
ADSL_TX
ADSL_RX
TROM
PA14
PA15
R56 10K
R73 10K
R69 10K
R70 10K_DNP
R72 10K
R22 1K_DNP
R21 1K
R19 1K_DNP
R23 1K_DNP
J2
2x2 HEADER
GREEN = DATA MODE
YELLOW = TRAINING
D9
D10
620075, GREEN
620077, YELLOW
R51 301
R71 301
U6B
MTC-20156TB-I
U6A
MTC-20156TB-I
UTP_RX_SOC
UTP_RX_CLAV
UTP_TX_CLAV
UTP_RX_CLK
UTP_TX_CLK
R40 10K_DNP
R39 10K
R33 10K
R31 68
R38 68
C52 0.01u 25V
C51 0.01u 25V
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Title
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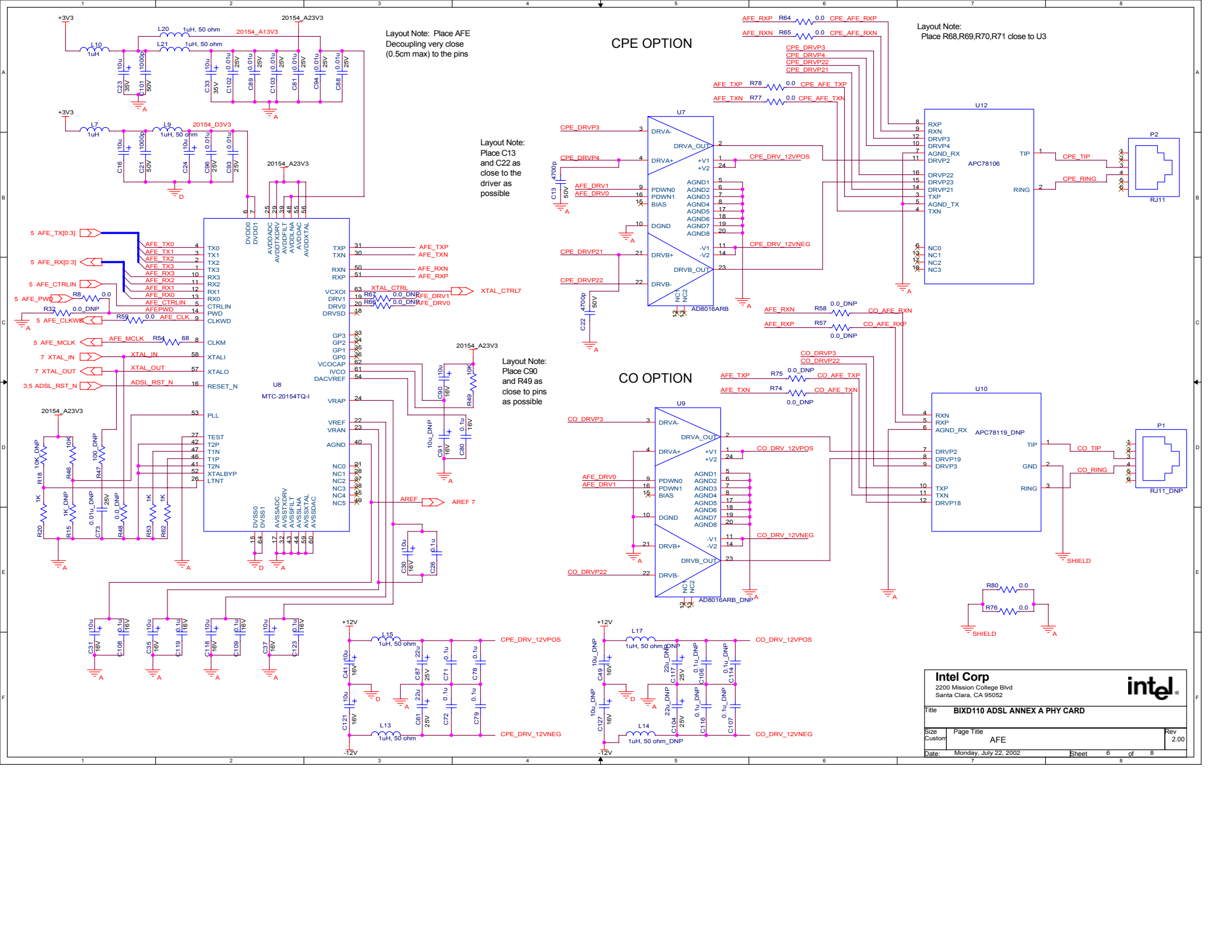
Layout Note: Place AFE Decoupling very close (0.5cm max) to the pins
Layout Note: Place C13 and C22 as close to the driver as possible
Layout Note: Place C90 and R49 as close to pins as possible
CPE OPTION
CO OPTION
Layout Note: Place R68,R69,R70,R71 close to U3
MTC-20154TQ-I
AD8016ARB
AD8016ARB_DNP
APC78106
APC78119_DNP
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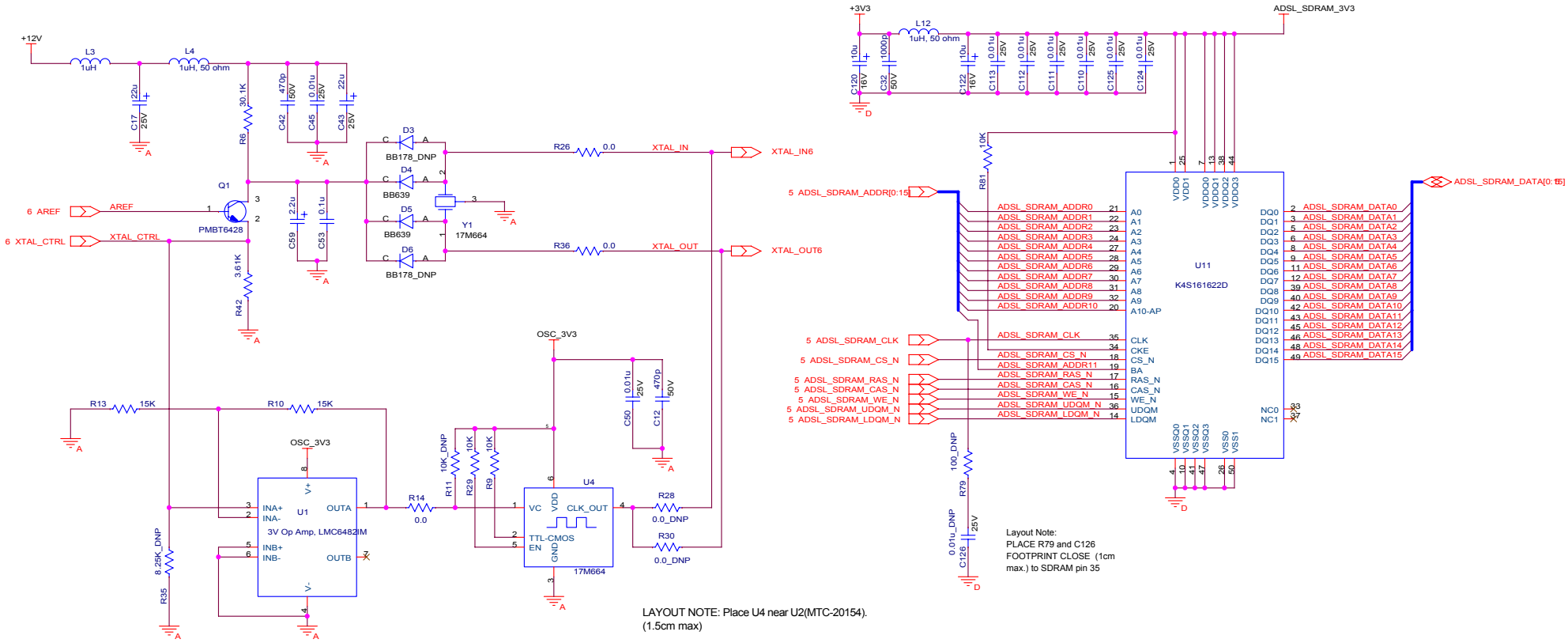

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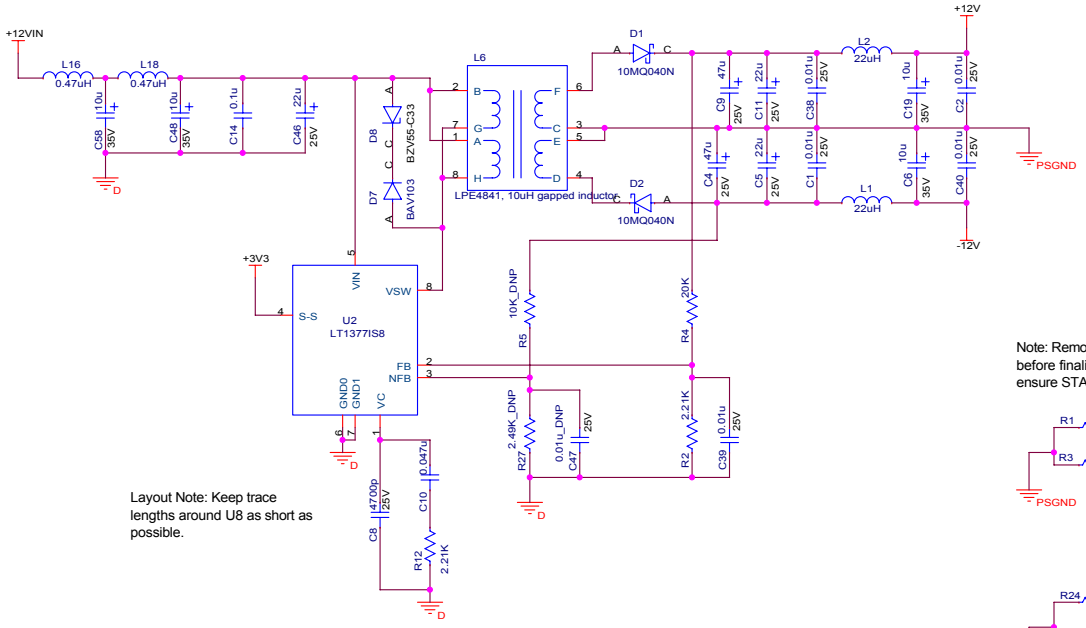
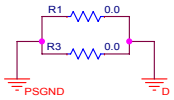
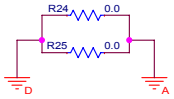


Layout Note: Keep trace lengths around U8 as short as possible.

Layout Note: Route "PSGND" net separately from "GND" net. "PSGND" net has to be a wide track, but not a plane.

Note: Remove R1 and R3 before finalizing layout. These ensure STAR Distribution.

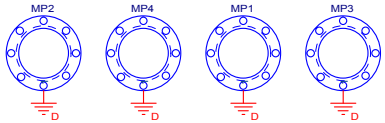




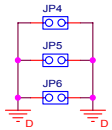
Note: R24 and R25 are the connection points from AGND to DGND.

Layout Note: Place both resistors side by side and add large copper bonding area to allow at least 5 vias.

The Grounded mounting holes,MP1-MP4, are to be placed in the four corners of the board.



Silkscreen:



GND

GND

GND

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