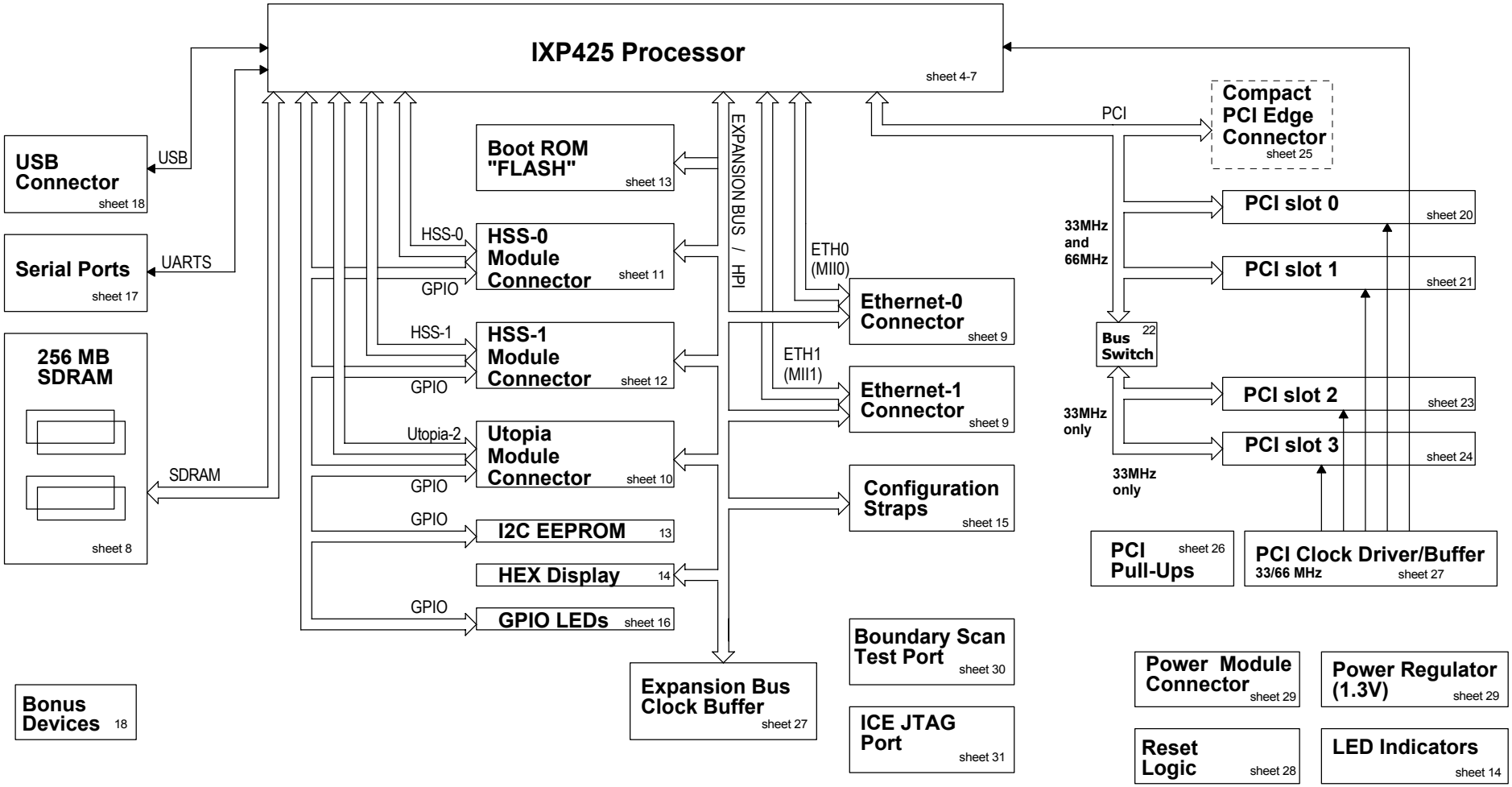
BIXMB425BD (REV A4) Base Card



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
Size B	Page Title: Title Page / Block Diagram	Rev 1.2
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SCHEMATIC ANNOTATIONS

VOLTAGE RAILS

+12V	Received through power connector. Supplied to PCI slots, Utopia, HSS0, HSS1, and ethernet modules.
+5V	Received through power connector. Supplied to PCI slots and the Utopia, HSS0, HSS1, and ethernet modules.
+5V_USB	Received on USB port and used for USB line pull-up.
+3V3	Received through power connector. Supplied to PCI slots, flash, I2C EEPROM, serial ports, SDRAM, and the Utopia, HSS0, HSS1, and ethernet modules.
+3V3_CJ	Derived from the +3V3 rail to allow power measurement on IXP425. Supplied to IXP425 processor.
+2V5	Received through power connector. Supplied to Utopia, HSS0, HSS1, and ethernet modules.
+1V3	Derived from the +3V3 rail. Used by the IXP425 processor.
-64V	Received through power connector. Supplied to HSS0, HSS1, and ethernet modules.
-32V	Received through power connector. Supplied to HSS0, HSS1, and ethernet modules.

GROUNDS

GND_DIGITAL	Digital Ground Plane

DESIGN NOTES

0.0 ohm resistors are placed to allow accessiblity to nodes that may be of interest.

_DNP	Do Not Populate this component if this designation is found on component's schematic.

REVISION HISTORY

Rev 1.00	* Original Release (Rev A2 Base Card)
Rev 1.10	* Updated IXP425 pin D25 pull-down resistor. (Rev A3 Base Card)
Rev 1.20	* Added Design Notes for JTAG. Changed circuitry for PWRON_RST_N. Added power sequencing circuit. (Rev A4 Base Card)

RELATED DOCUMENTATION

	DOCUMENT #
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Hardware Design Guidelines	252817
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Specification Update	252702
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Datasheet	252479
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual	252480
Intel® IXP400 Software Specification Update	273795
Intel® IXP400 Software Programmer's Guide	252539
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors: I2C Implementation Using the GPIO Pins	252137
Intel® LXT971A/972A 3.3V PHY Transceivers Design and Layout Guide Application Note	249016
Intel® IXDP425 / IXCDP1100 Development Platform Schematics	N/A

Note: Documentation is available on developer.intel.com

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These schematics may not reflect some versions of the manufactured board. Contact your Intel representative for details.

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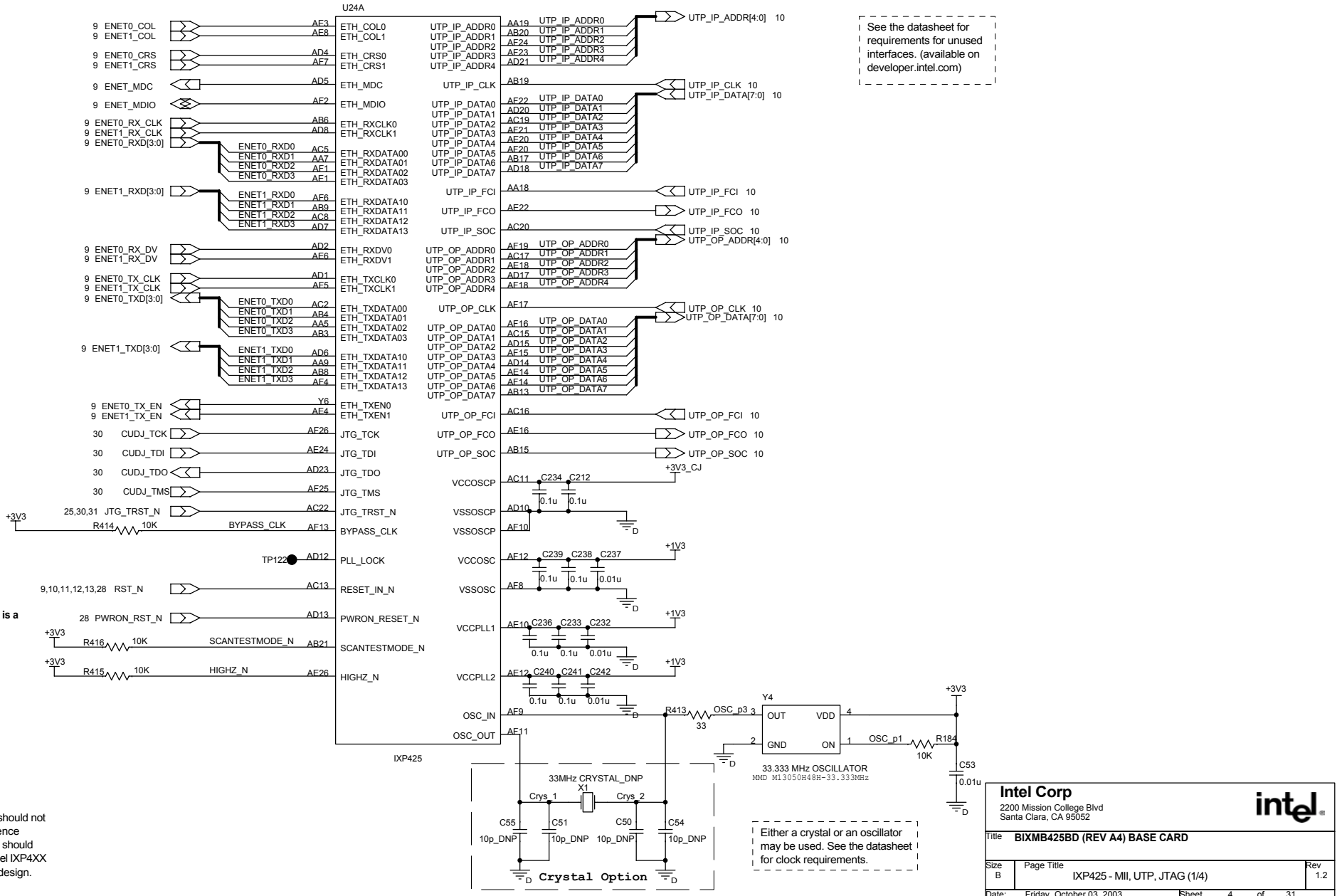
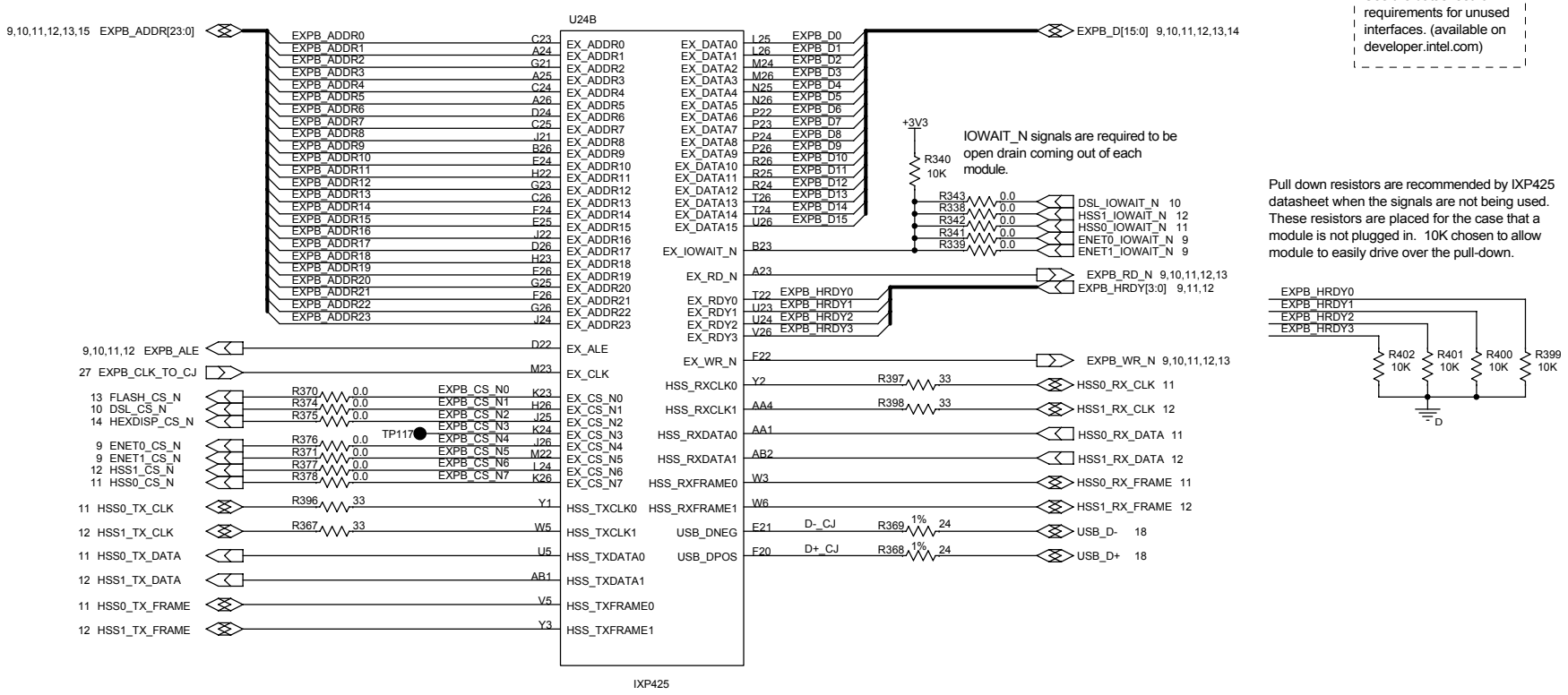
Title **BIXMB425BD (REV A4) BASE CARD**

Size	Page Title	Rev
Custom	Schematic Notes	1.2

Date: Friday, October 03, 2003 Sheet 3 of 31



Intel Corp	2200 Mission College Blvd, Santa Clara, CA 95052
Title	BIXMB425BD (REV A4) BASE CARD
Size	B
Page Title	IXP425 - MII, UTP, JTAG (1/4)
Rev	1.2
Date:	Friday, October 03, 2003
Sheet	4 of 31



See the datasheet for requirements for unused interfaces. (available on developer.intel.com)

Pull down resistors are recommended by IXP425 datasheet when the signals are not being used. These resistors are placed for the case that a module is not plugged in. 10K chosen to allow module to easily drive over the pull-down.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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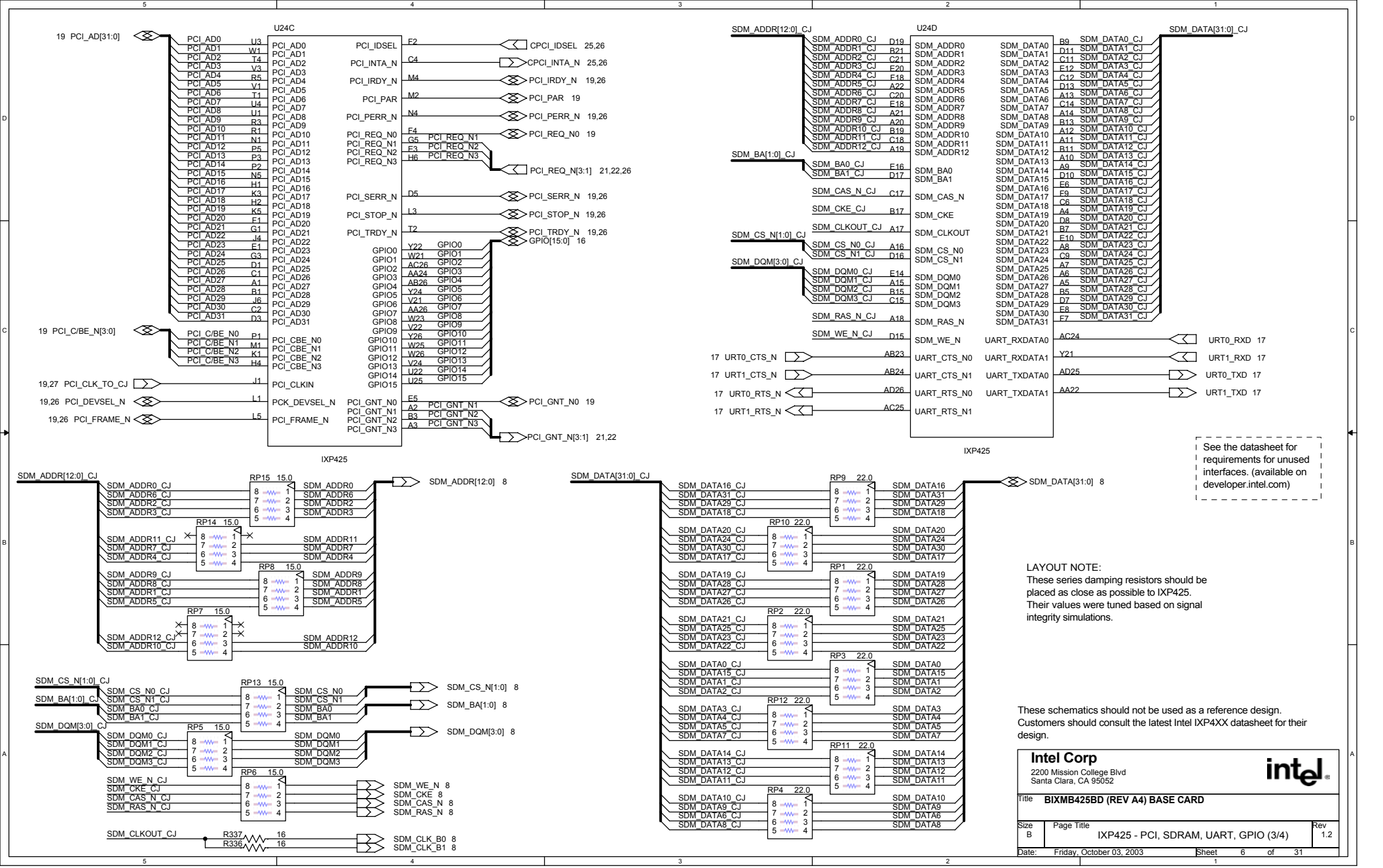
Title: **BIXMB425BD (REV A4) BASE CARD**

Size	Page Title	Rev
B	IXP425 - EXPB, HSS (2/4)	1.2

Date: Friday, October 03, 2003 Sheet 5 of 31


U24C
IXP425
U24D
IXP425
See the datasheet for requirements for unused interfaces. (available on developer.intel.com)
LAYOUT NOTE:
These series damping resistors should be placed as close as possible to IXP425. Their values were tuned based on signal integrity simulations.
These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.
Intel Corp
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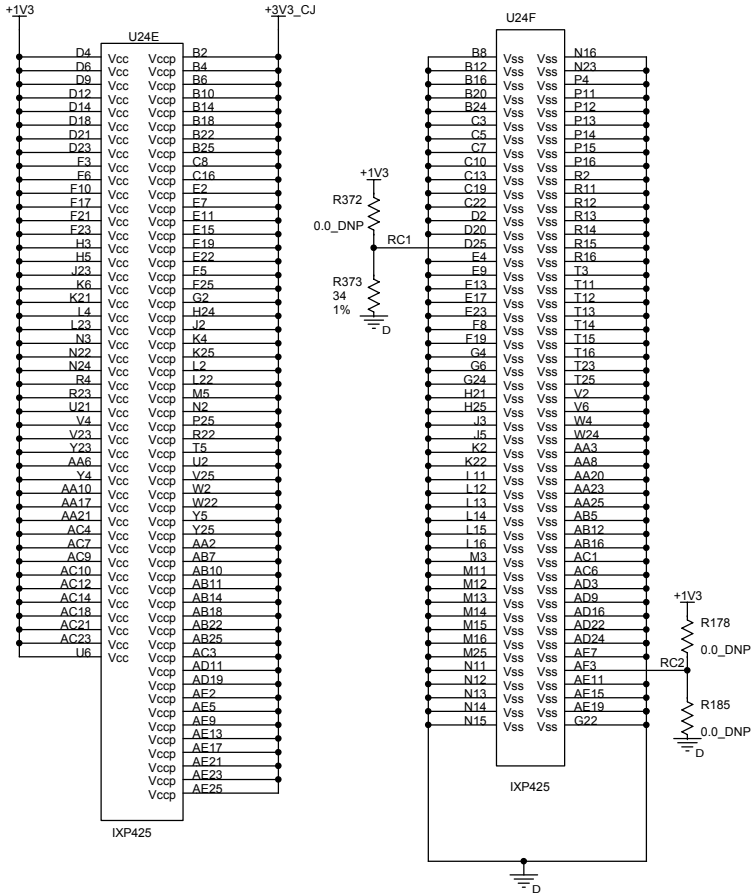
Title BIXMB425BD (REV A4) BASE CARD
Size B
Page Title IXP425 - PCI, SDRAM, UART, GPIO (3/4)
Rev 1.2
Date: Friday, October 03, 2003
Sheet 6 of 31

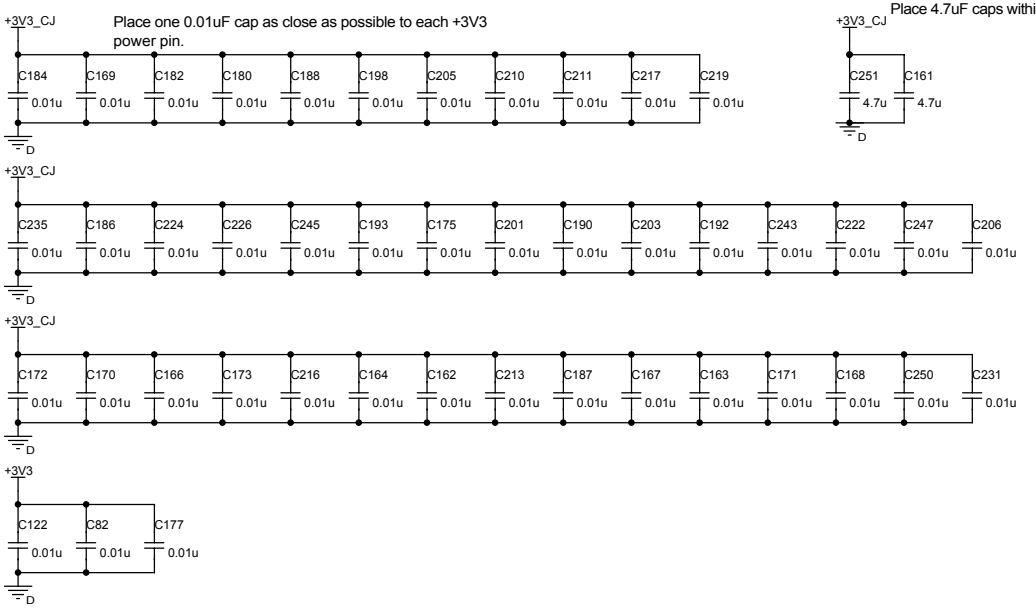


Pin AF3 is reserved. For pin D25, a 34 ohm, 1% resistor must be populated.

I/O Decoupling

Place one 0.01uF cap as close as possible to each +3V3 power pin.

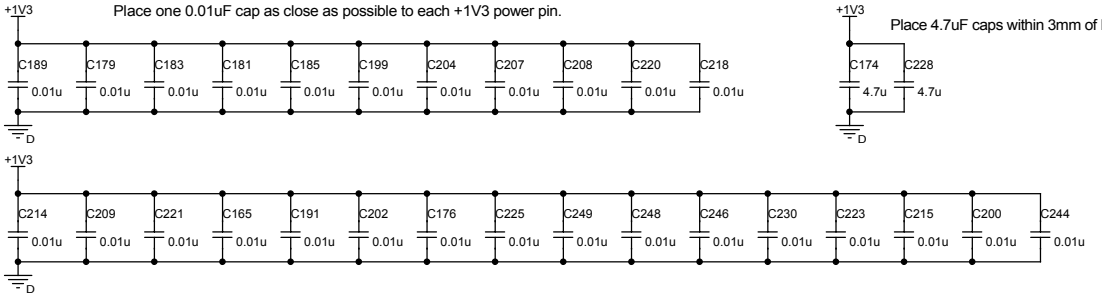
Place 4.7uF caps within 3mm of IXP425



Core Decoupling

Place one 0.01uF cap as close as possible to each +1V3 power pin.

Place 4.7uF caps within 3mm of IXP425



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: IXP425 - Vcc, Vccp, Vss (4/4)	Rev 1.2
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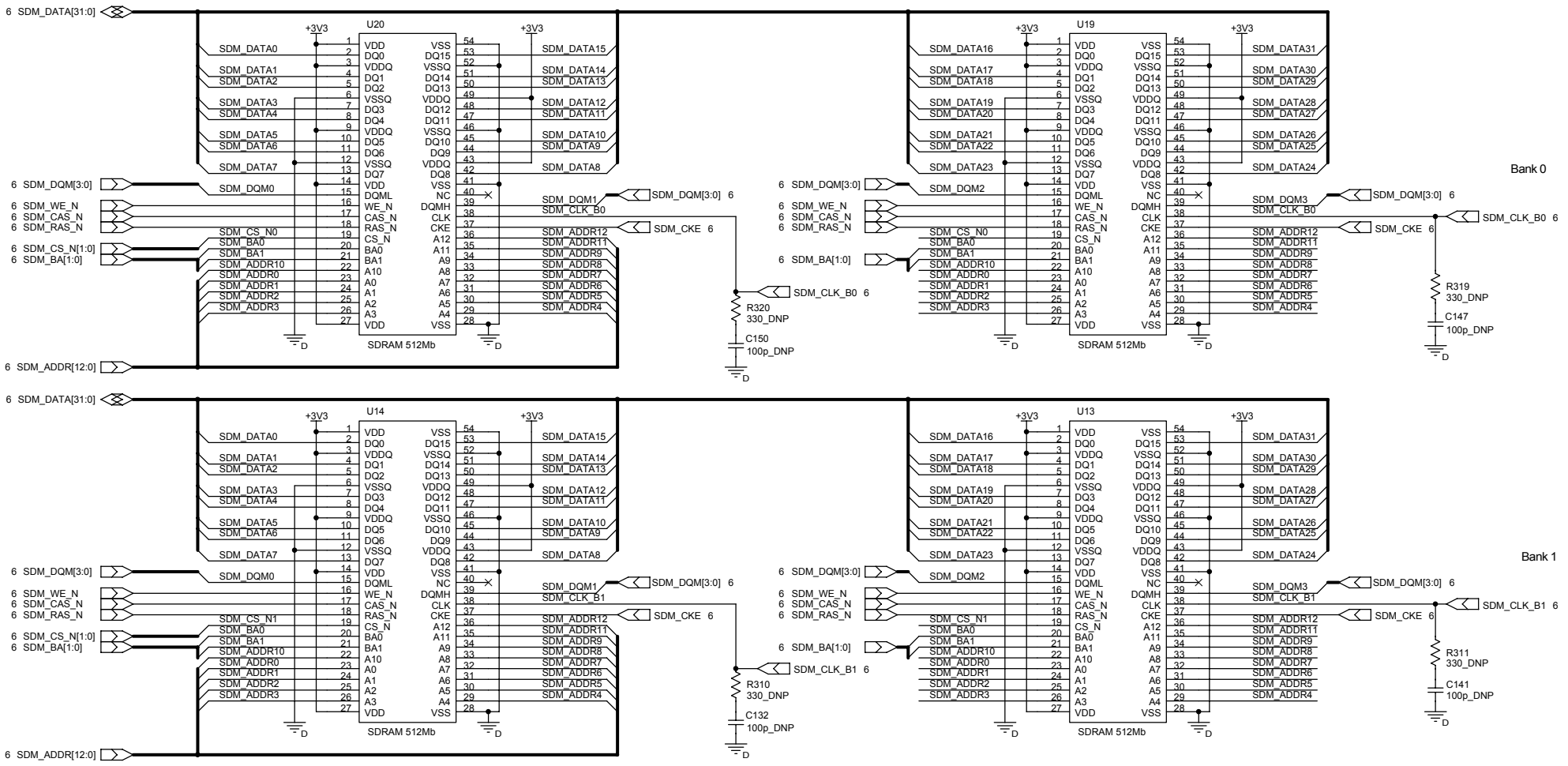
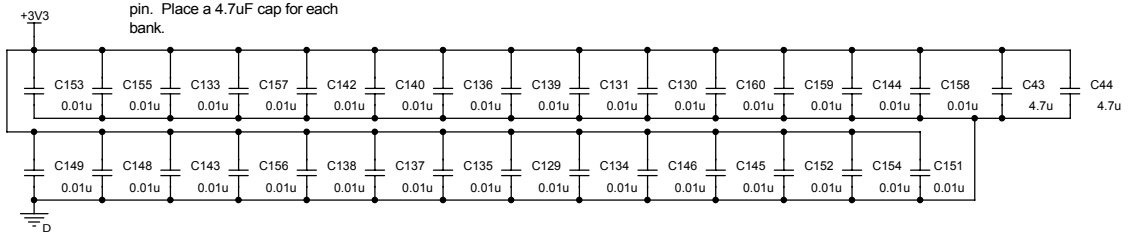


Place a 0.01uF cap by each power pin. Place a 4.7uF cap for each bank.



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

Refer to the Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Datasheet for the supported memory configurations.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: 256MByte SDRAM	Rev 1.2
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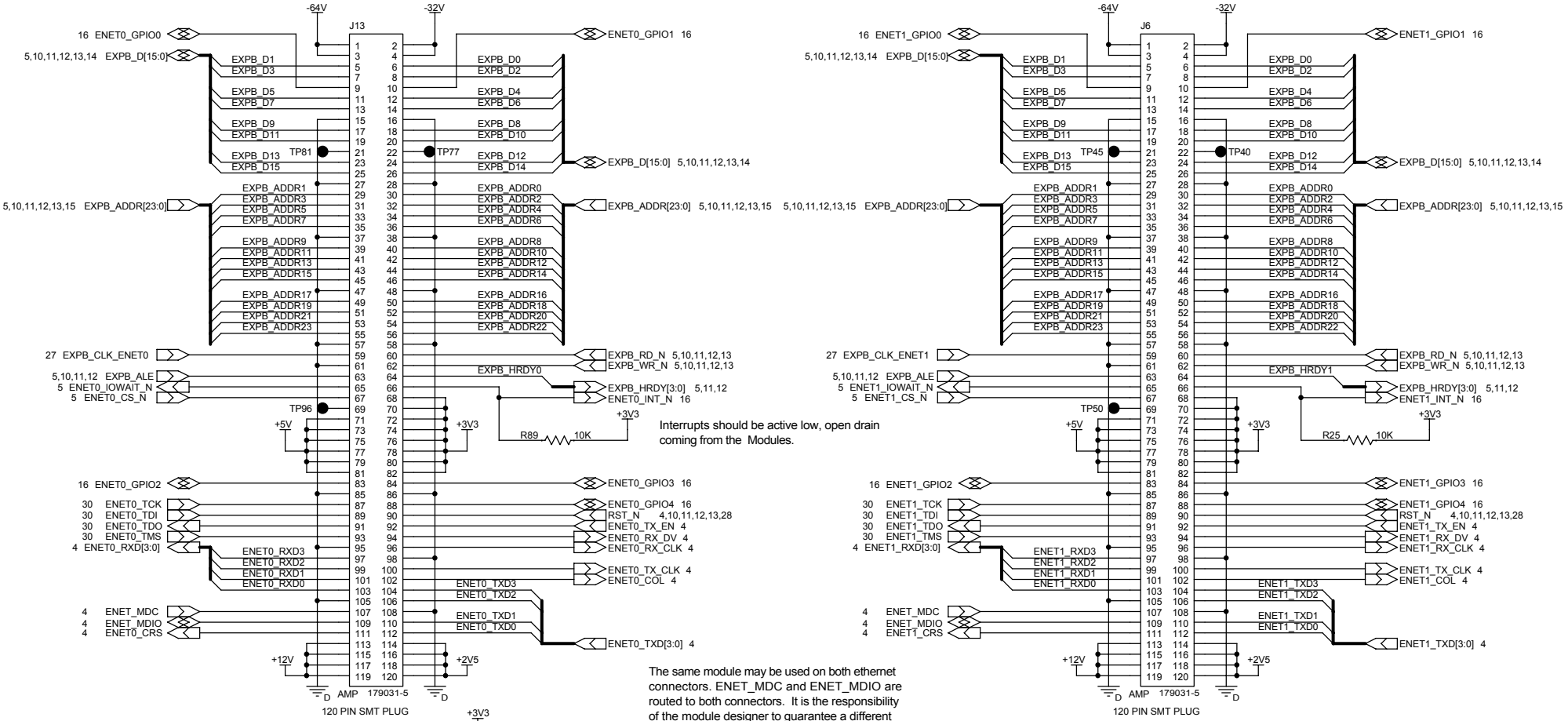
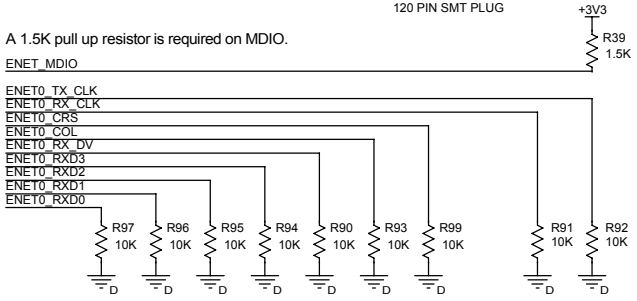
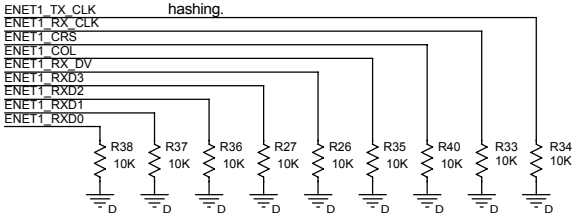


Interrupts should be active low, open drain coming from the Modules.

The same module may be used on both ethernet connectors. ENET_MDC and ENET_MDIO are routed to both connectors. It is the responsibility of the module designer to guarantee a different address on each connector.
ENET1 has ethernet MAC hashing.
ENET0 does not have ethernet MAC hashing.

A 1.5K pull up resistor is required on MDIO.





Pull down resistors are recommended by IXP4XX datasheet when the signals are not being used. These resistors are placed for the case that a ethernet module is not plugged in. 10K chosen to allow the module to easily drive over the pull-down.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title: **BIXMB425BD (REV A4) BASE CARD**

Size	Page Title	Rev
B	Ethernet Connectors	1.2

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5,9,11,12,13,15 EXPB_ADDR[23:0]

DESIGN NOTE:
Any one of the stackable Utopia modules can generate an interrupt to the IXP4XX. The interrupts should be active low, open drain coming from the modules.

+3V3 R179 10K

16 DSL_INT_N

+12V +12V

J15

EXPB_ADDR0 EXPB_ADDR2 EXPB_ADDR1 EXPB_ADDR3 EXPB_ADDR4 EXPB_ADDR6 EXPB_ADDR8 EXPB_ADDR5 EXPB_ADDR7 EXPB_ADDR9

5,9,11,12,13,14 EXPB_D[15:0]

EXPB_D0 EXPB_D1 EXPB_D2 EXPB_D4 EXPB_D3 EXPB_D5 EXPB_D6 EXPB_D7

EXPB_CLK_UTP 27
EXPB_D[15:0] 5,9,11,12,13,14

16 UTP_GPIO0
5,9,11,12,13 EXPB_WR_N
16 UTP_GPIO2
4,9,11,12,13,28 RST_N

UTP_GPIO1 16
EXPB_RD_N 5,9,11,12,13
GASP_INT_N 29
DSL_CS_N 5

5,9,11,12 EXPB_ALE
30 DSL_TDI
30 DSL_TDO

+3V3 +3V3

30 DSL_TCK

+2V5 +2V5

DSL_TMS 30

5,9,11,12,13,15 EXPB_ADDR[23:0]

EXPB_ADDR21 EXPB_ADDR22

DSL_IOWAIT_N 5

EXPB_ADDR23

UTP_IP_CLK

4 UTP_IP_DATA[7:0]

UTP_IP_DATA1 UTP_IP_DATA0 UTP_IP_DATA2 TP118

UTP_OP_CLK
UTP_OP_DATA2
UTP_OP_DATA[7:0] 4
UTP_OP_FCO 4

4 UTP_IP_FCI
4 UTP_OP_DATA[7:0]

UTP_OP_DATA7 UTP_OP_DATA4 UTP_OP_DATA6

UTP_OP_DATA0 UTP_OP_DATA1 UTP_OP_DATA3 UTP_OP_DATA5

UTP_IP_DATA7 UTP_IP_DATA3 UTP_IP_DATA5

UTP_OP_FCI 4
UTP_OP_SOC 4
UTP_IP_DATA[7:0] 4

UTP_IP_DATA4 UTP_IP_DATA6

4 UTP_IP_SOC
4 UTP_IP_FCO
4 UTP_IP_ADDR[4:0]

UTP_GPIO3 16
UTP_OP_ADDR[4:0] 4

UTP_IP_ADDR4 UTP_IP_ADDR3 UTP_OP_ADDR4 UTP_OP_ADDR3 UTP_OP_ADDR2

UTP_IP_ADDR2 UTP_IP_ADDR1 UTP_IP_ADDR0 UTP_OP_ADDR1 UTP_OP_ADDR0

16 UTP_GPIO4

UTP_GPIO5 16

+5V +5V

AMP 5-179010-5
120 PIN SMT RECEPTACLE

Pull down resistors are recommended by IXP425 datasheet when the signals are not being used. These resistors are placed for the case that a Utopia PHY is not plugged in. 10K chosen to allow Utopia module to easily drive over the pull-down.

UTP_OP_FCI
UTP_IP_FCI
UTP_IP_SOC
UTP_IP_DATA0
UTP_IP_DATA1
UTP_IP_DATA2
UTP_IP_DATA3
UTP_IP_DATA4
UTP_IP_DATA5
UTP_IP_DATA6
UTP_IP_DATA7

R128 10K R122 10K R126 10K R123 10K R127 10K R151 10K R153 10K R152 10K R125 10K R129 10K R124 10K

5,9,11,12,13,14 EXPB_D[15:0]

J14

EXPB_D8 EXPB_D9
EXPB_D10 EXPB_D11
TP116 TP112
EXPB_D12 EXPB_D13
EXPB_D14 EXPB_D15
TP115 TP111
EXPB_ADDR10 EXPB_ADDR11
EXPB_ADDR12 EXPB_ADDR13
TP114 TP110
EXPB_ADDR14 EXPB_ADDR15
EXPB_ADDR16 EXPB_ADDR17
TP113 TP109
EXPB_ADDR18 EXPB_ADDR19
EXPB_ADDR20
TP103 TP108 TP102

AMP 5-179010-1

5,9,11,12,13,15 EXPB_ADDR[23:0]

40 PIN SMT RECEPTACLE

All expansion bus address and data signals that are not placed on the main connector are passed through the 40-pin connector. Most Utopia modules will not use these signals.

Shunt 1-2 to enable oscillator (default).
Shunt 2-3 to disable oscillator.
Oscillator should be disabled in the case that the clock is supplied through the module.

+3V3 C197 0.1u

+3V3 JP12 UTP_CLK_EN

Y3 VDD OUT STAND-BY GND

33MHz OSCILLATOR

UTP_CLK R149 33 R147 33

Pull down resistors on Utopia clocks should be populated if no oscillators are driving the clock.

R150 10K_DNP R148 10K_DNP

UTP_IP_CLK
UTP_IP_CLK 4
UTP_OP_CLK 4
UTP_OP_CLK

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Size B	Page Title: Utopia-2 Connector	Rev 1.2
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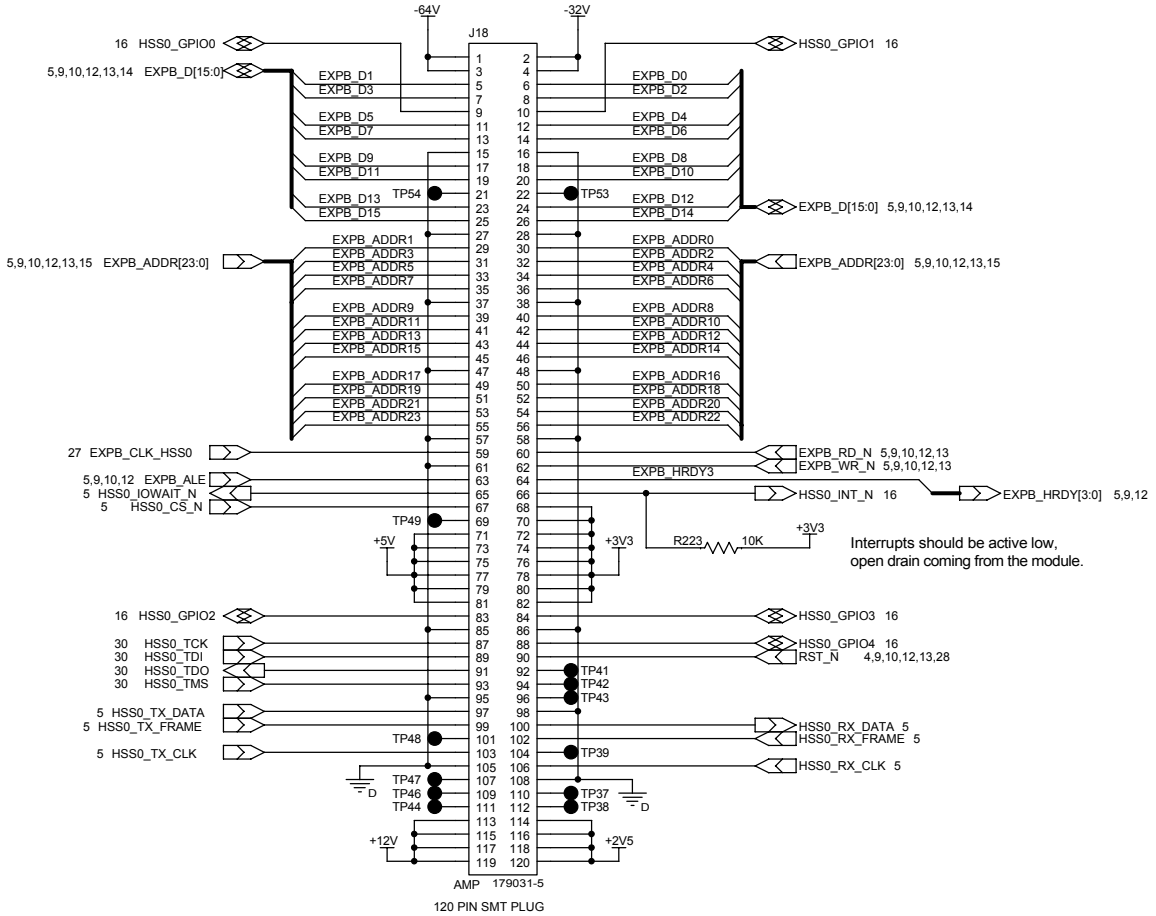
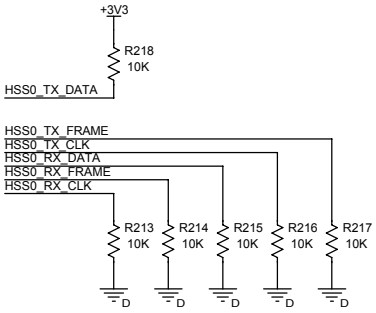


Resistors are recommended by IXP4XX datasheet when the signals are not being used. These resistors are placed for the case that a module is not plugged in. 10K chosen to allow the module to easily drive over the pull-down.

Pull up on HSS0_TX_DATA is placed because it is an open drain output from the IXP425.



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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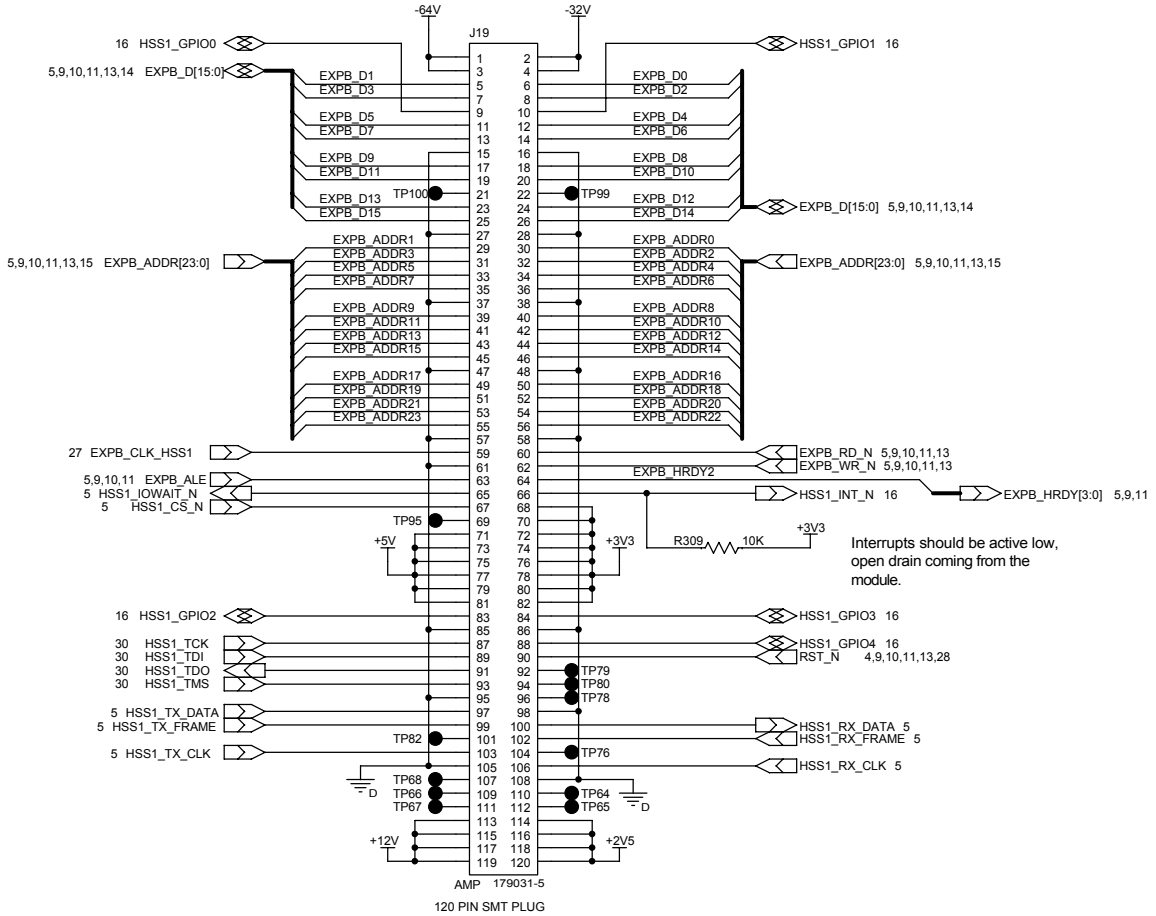
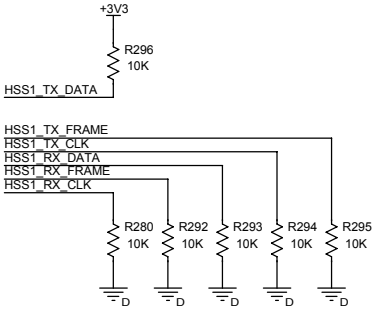
Title	**BIXMB425BD (REV A4) BASE CARD**	
Size: B	Page Title: HSS-0 Connector	Rev: 1.2
Date: Friday, October 03, 2003	Sheet 11 of 31	



Interrupts should be active low, open drain coming from the module.

Resistors are recommended by IXP4XX datasheet when the signals are not being used. These resistors are placed for the case that a module is not plugged in. 10K chosen to allow the module to easily drive over the pull-down.

Pull up on HSS1_TX_DATA is placed because it is an open drain output from the IXP425.



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title **BIXMB425BD (REV A4) BASE CARD**		
Size B	Page Title HSS-1 Connector	Rev 1.2
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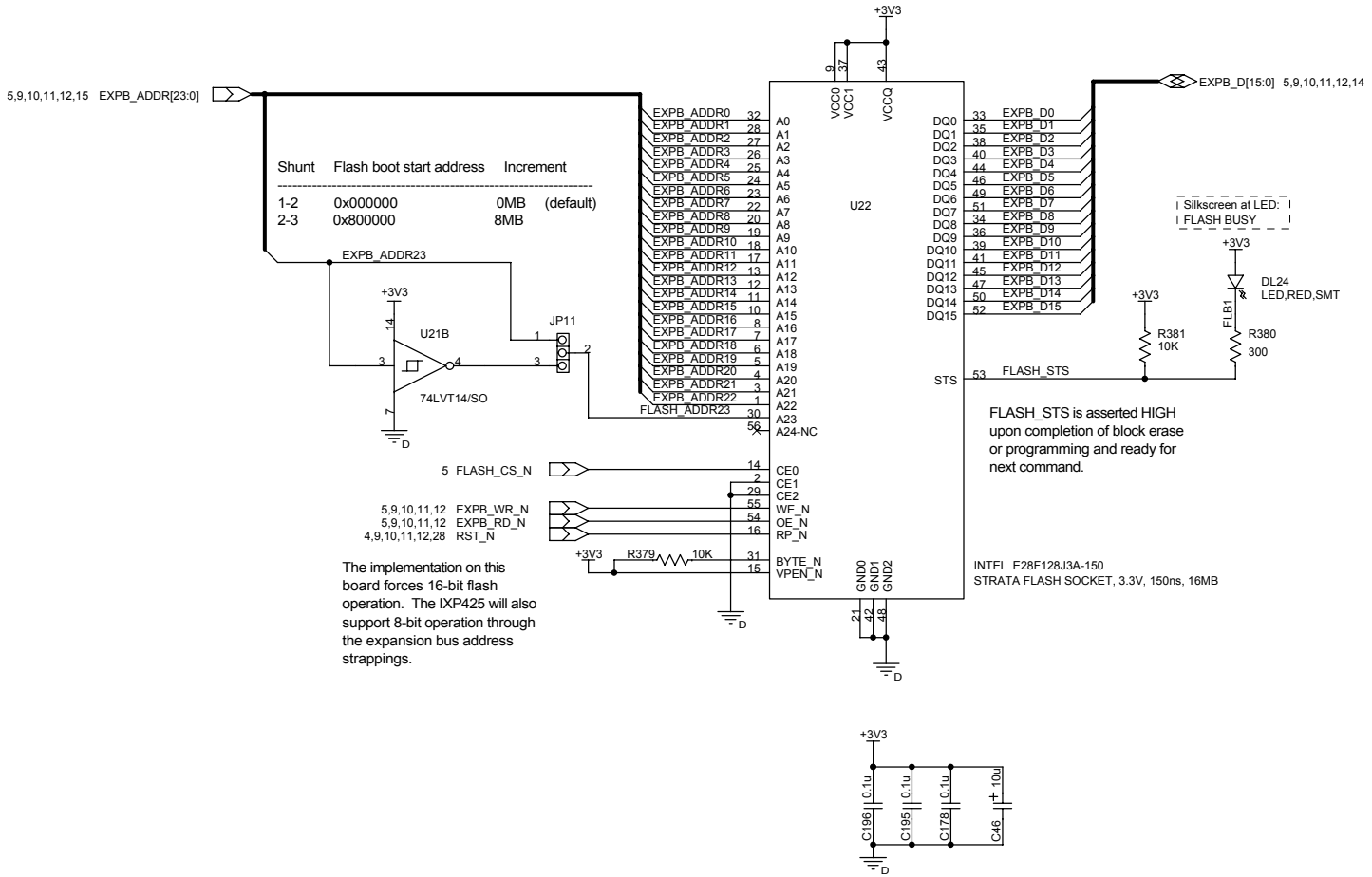
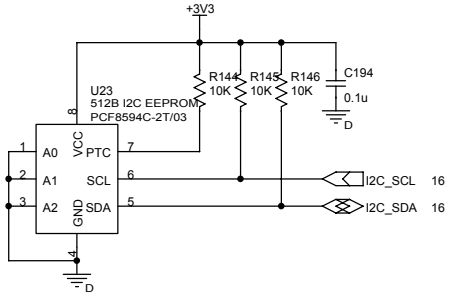
BOOT ROM



I2C EEPROM



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

Intel Corp 2200 Mission College Blvd Santa Clara, CA 95052		intel
Title **BIXMB425BD (REV A4) BASE CARD**		
Size B	Page Title BOOT ROM / I2C EEPROM	Rev 1.2
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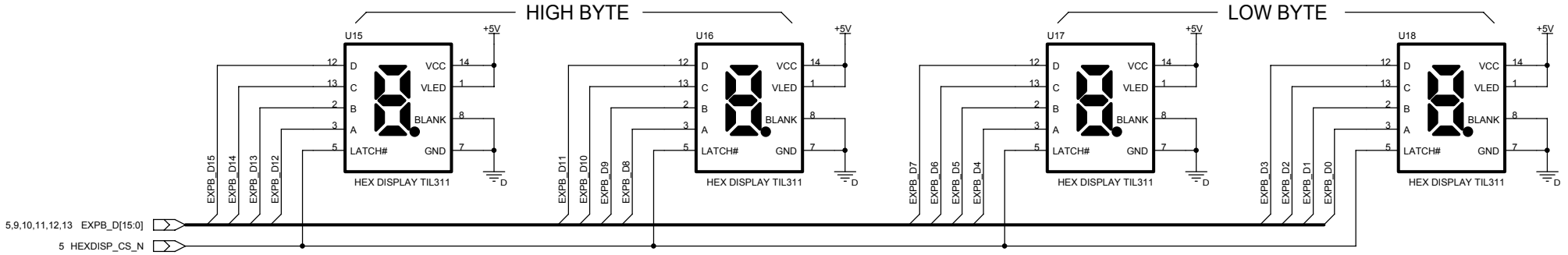
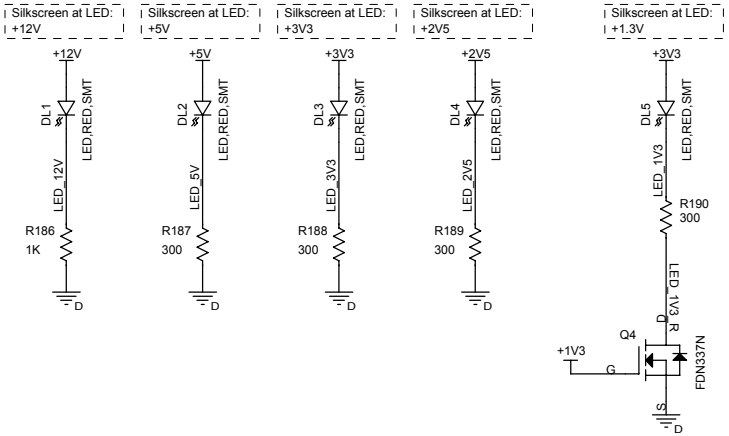
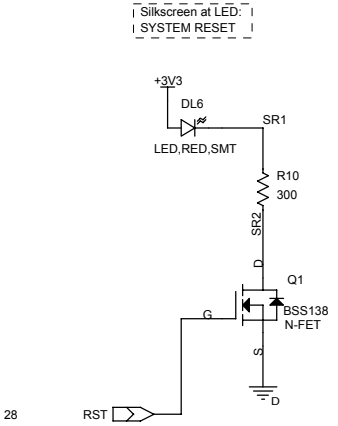
16-bit HEX Display for SW DEBUG



BOARD STATUS INDICATORS





These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size: B	Page Title: HEX Display / Board Status Indicators	Rev: 1.2
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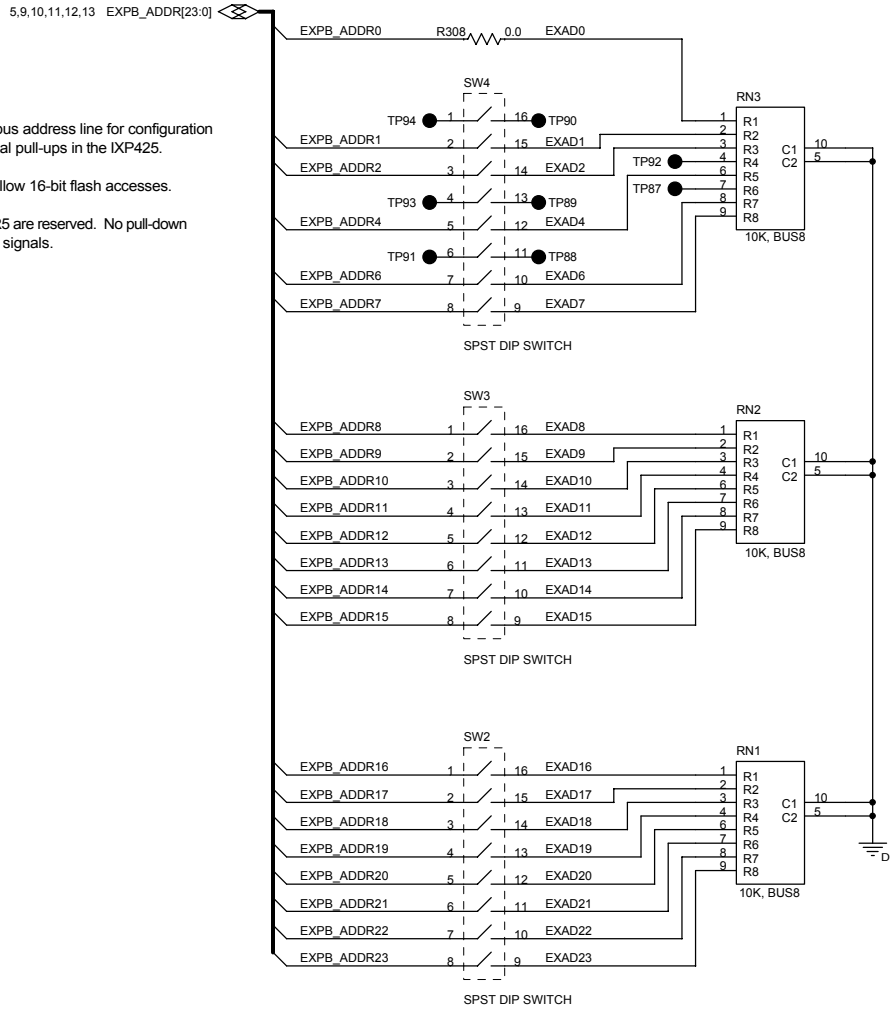
IXP425 CONFIGURATION STRAPS

"ON" pulls down the expansion bus address line for configuration purposes. There are weak internal pull-ups in the IXP425.

EXPB_ADDR0 is forced low to allow 16-bit flash accesses.

EXPB_ADDR3 and EXPB_ADDR5 are reserved. No pull-down resistor should be used on these signals.

See the developer's manual for expb_addr configuration options. (available on developer.intel.com)



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: Configuration Straps	Rev 1.2
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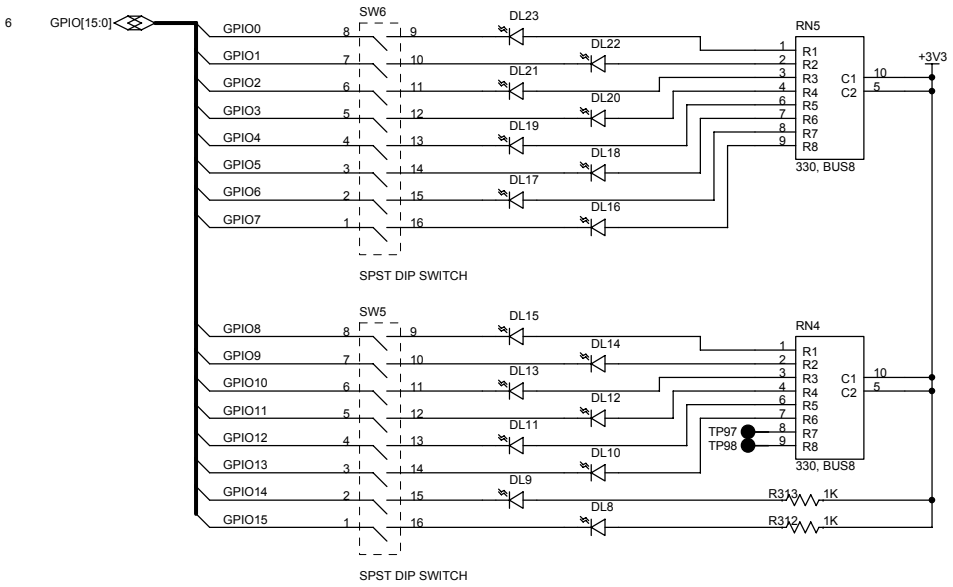
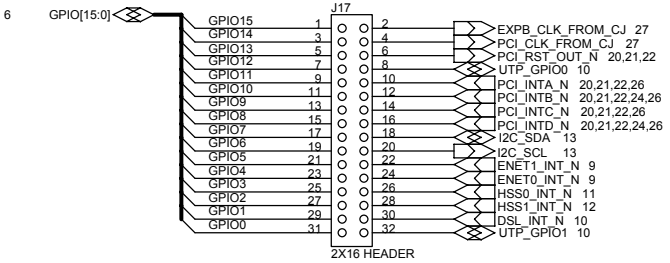
GPIO LEDs



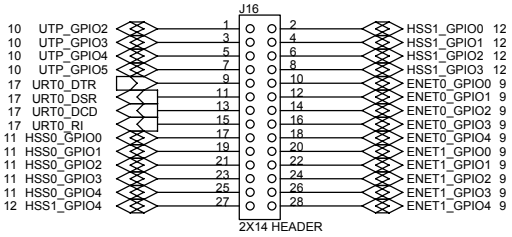
All GPIOs have 16 mA drive strength except GPIO14 and GPIO15 which have 8 mA current source / sink capability. This is because GPIO 14 and 15 have the alternate function of driving clocks.

Switches allow users the flexibility to choose whether to connect an LED to each GPIO as needed. "ON" connects the LED to the GPIO. Default configuration is GPIOs connected to LEDs (all switches in "ON" position).

GPIO Header A



GPIO Header B



Headers are placed to allow flexible routing of GPIOs to those places needed in a particular design.

To use default GPIO settings, shunt each pair of pins on GPIO Header A:
1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18, 19-20, 21-22, 23-24, 25-26, 27-28, 29-30, 31-32.
Nothing should be connected on GPIO Header B.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
Size B	Page Title: GPIO Routing and LEDs	Rev 1.2
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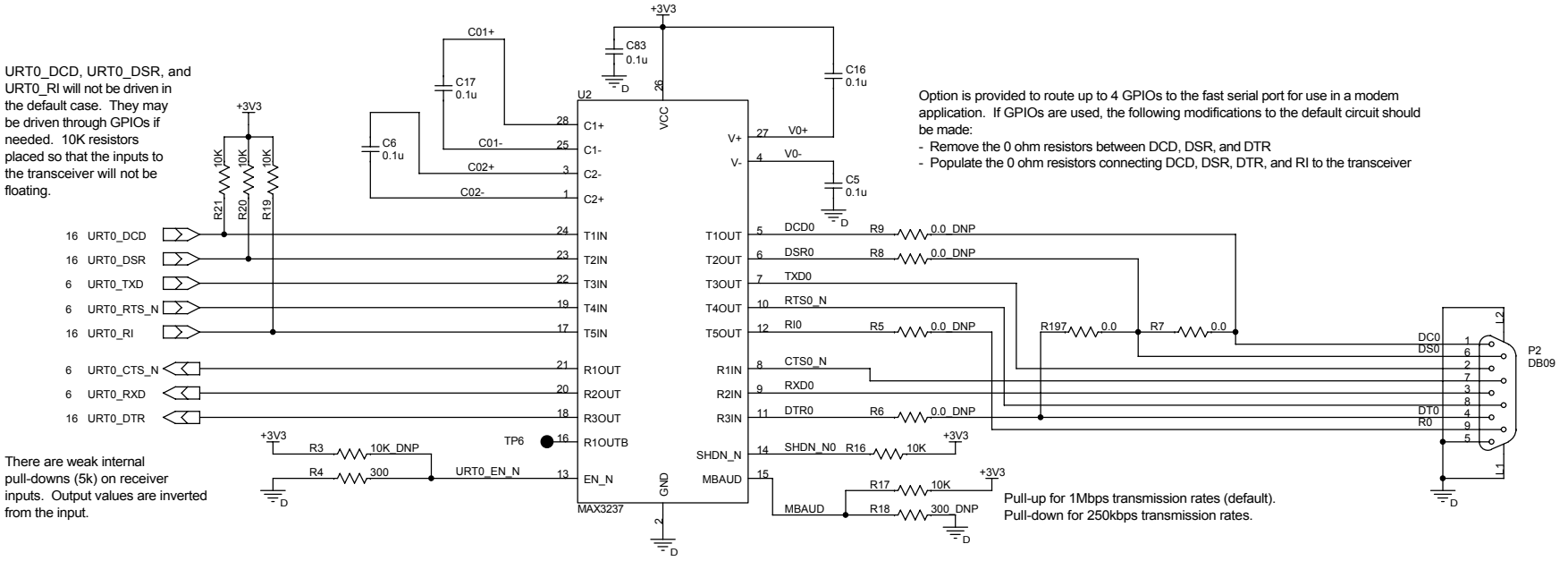
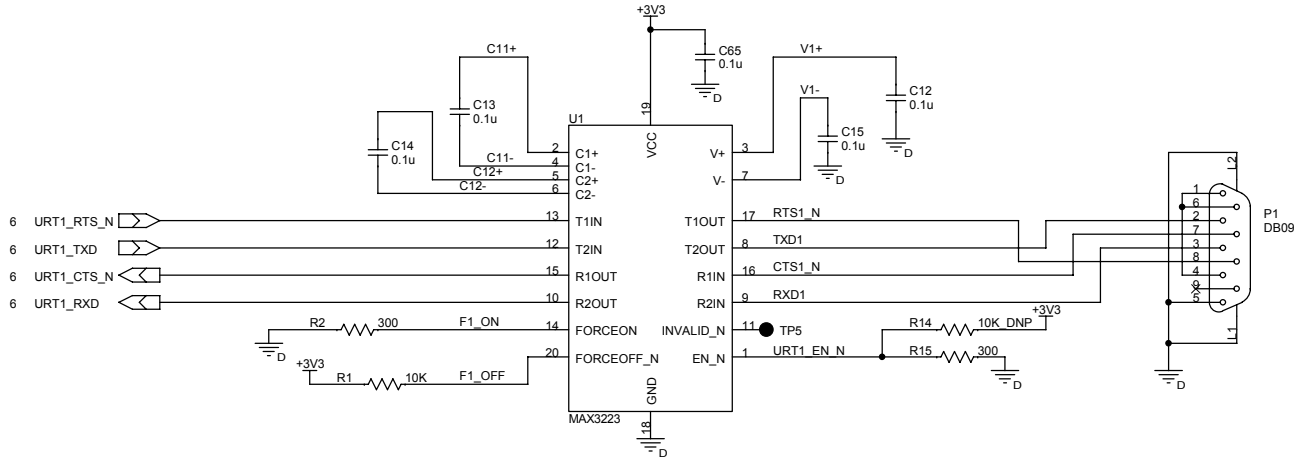
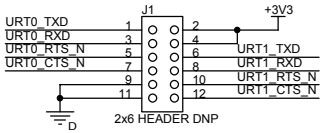
UART (FAST PORT)



UART (CONSOLE PORT)





These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: UART PORTS	Rev 1.2
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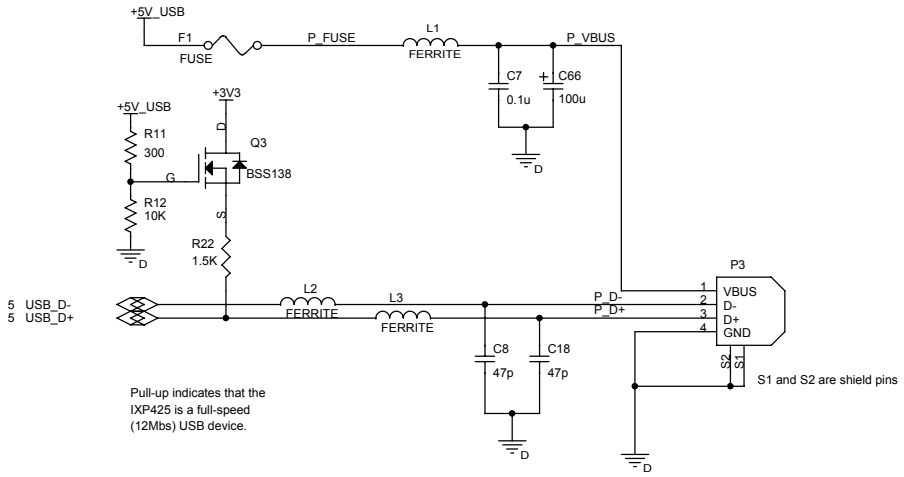
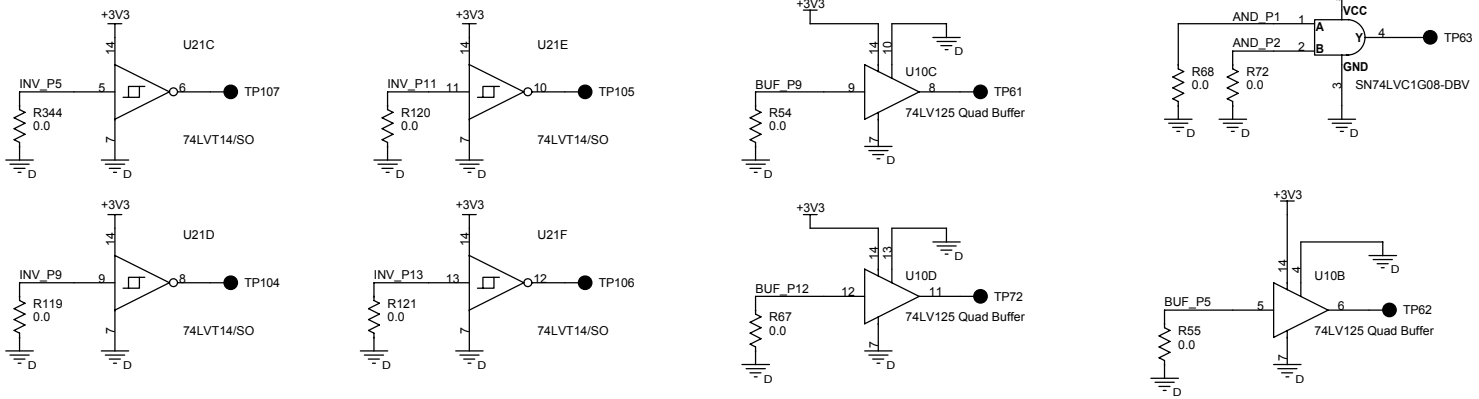
USB CONNECTOR



BONUS DEVICES



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: USB Connector / Bonus devices	Rev 1.2
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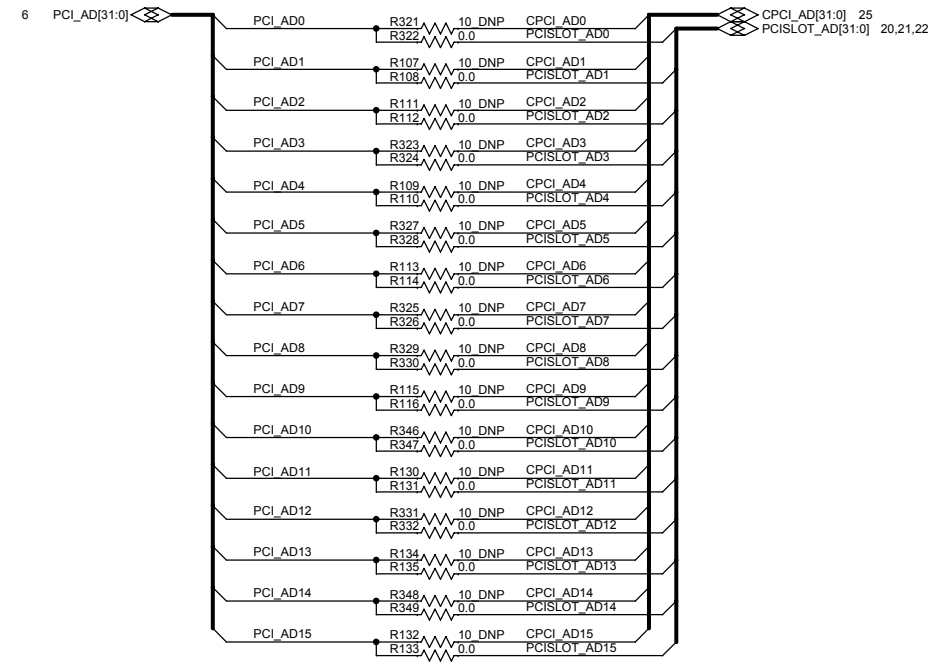

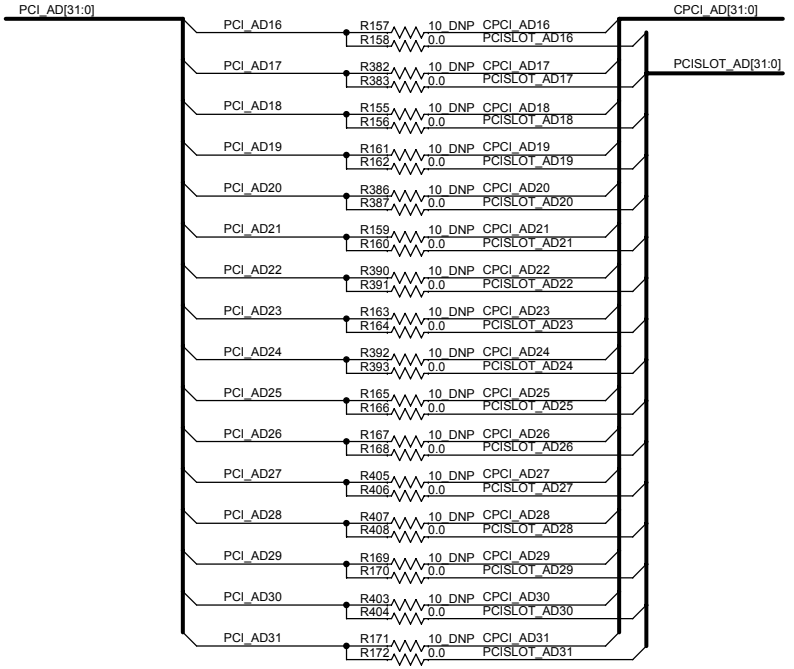

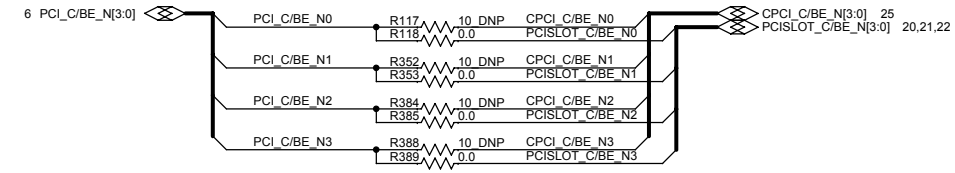

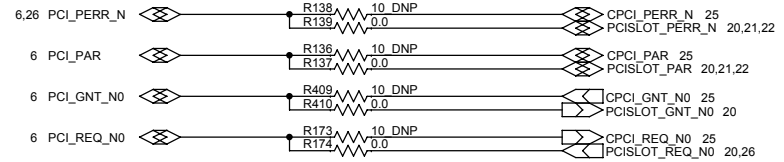

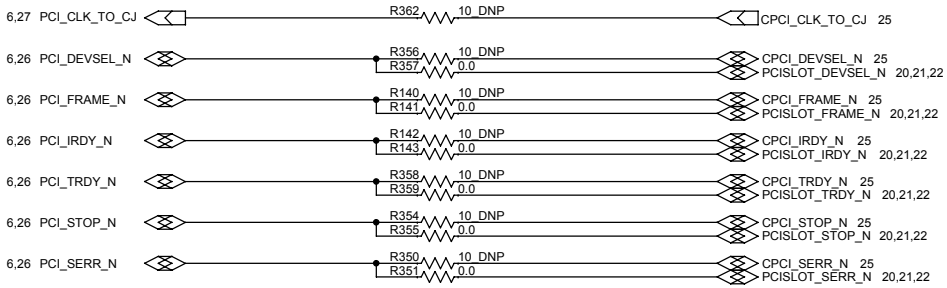

PCI signals must be routed exclusively to either the compact PCI connector or the PCI slots. Zero ohm resistors will be populated on only one of two signal paths. As shown, signals are routed to the PCI slots.

In order to configure the board as a compact PCI card, all resistors shown on this page to be stuffed must be unpopulated, and all unpopulated resistors shuld be stuffed. Also, the PCI slots and all associated circuitry must be unpopulated. A separate set of schematics will show this configuration.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: PCI Routing	Rev 1.2
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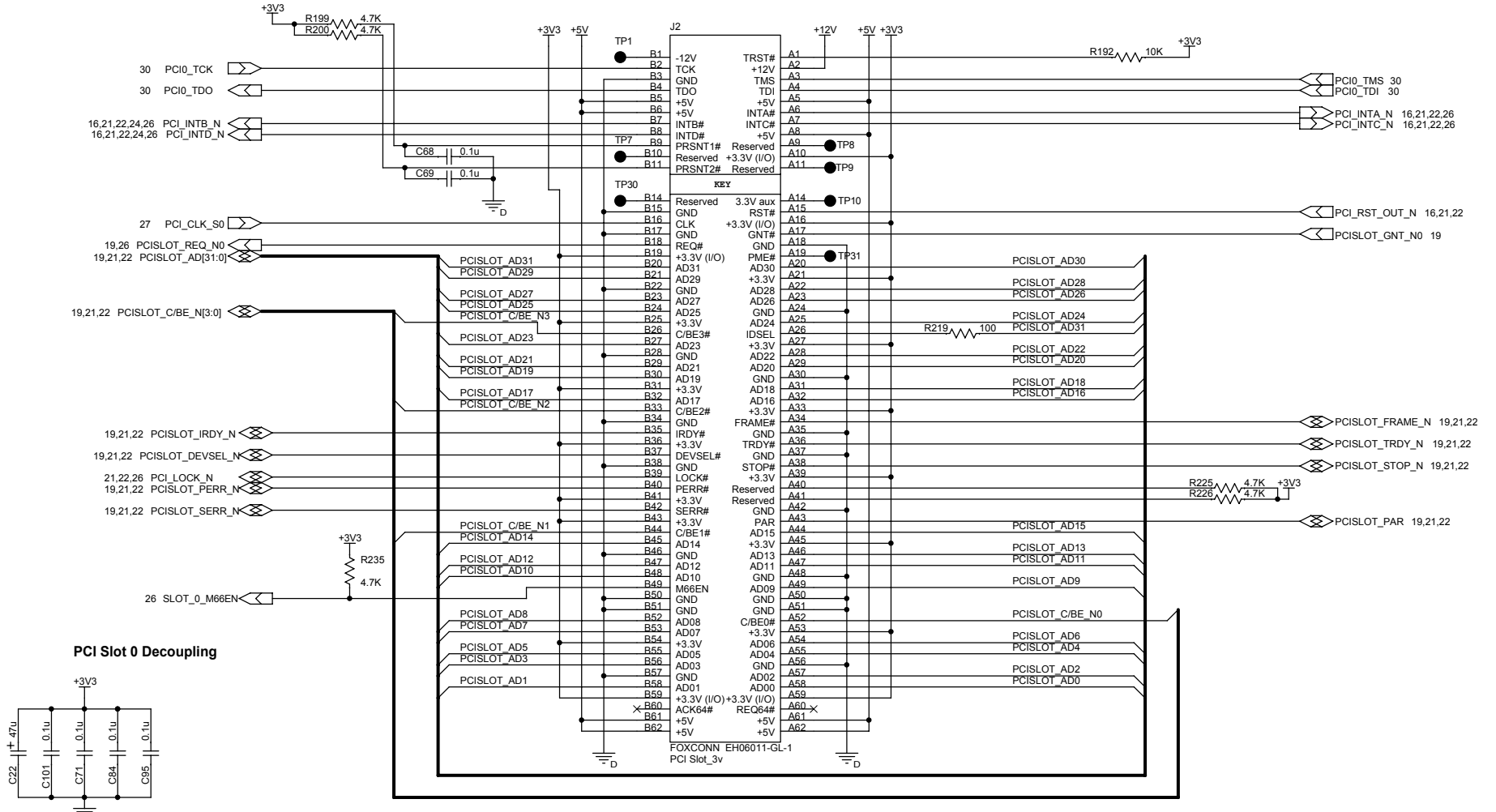
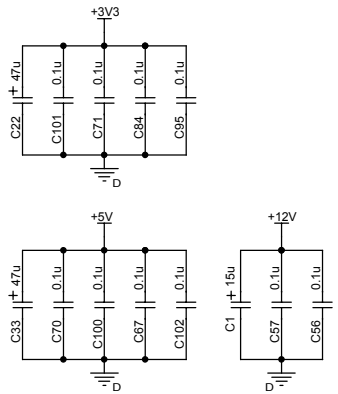


PCI Slot 0 Decoupling



If board is configured as a CPCI slot, none of the components on this page should be populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: PCI SLOT #0 (66 MHz capable)	Rev 1.2
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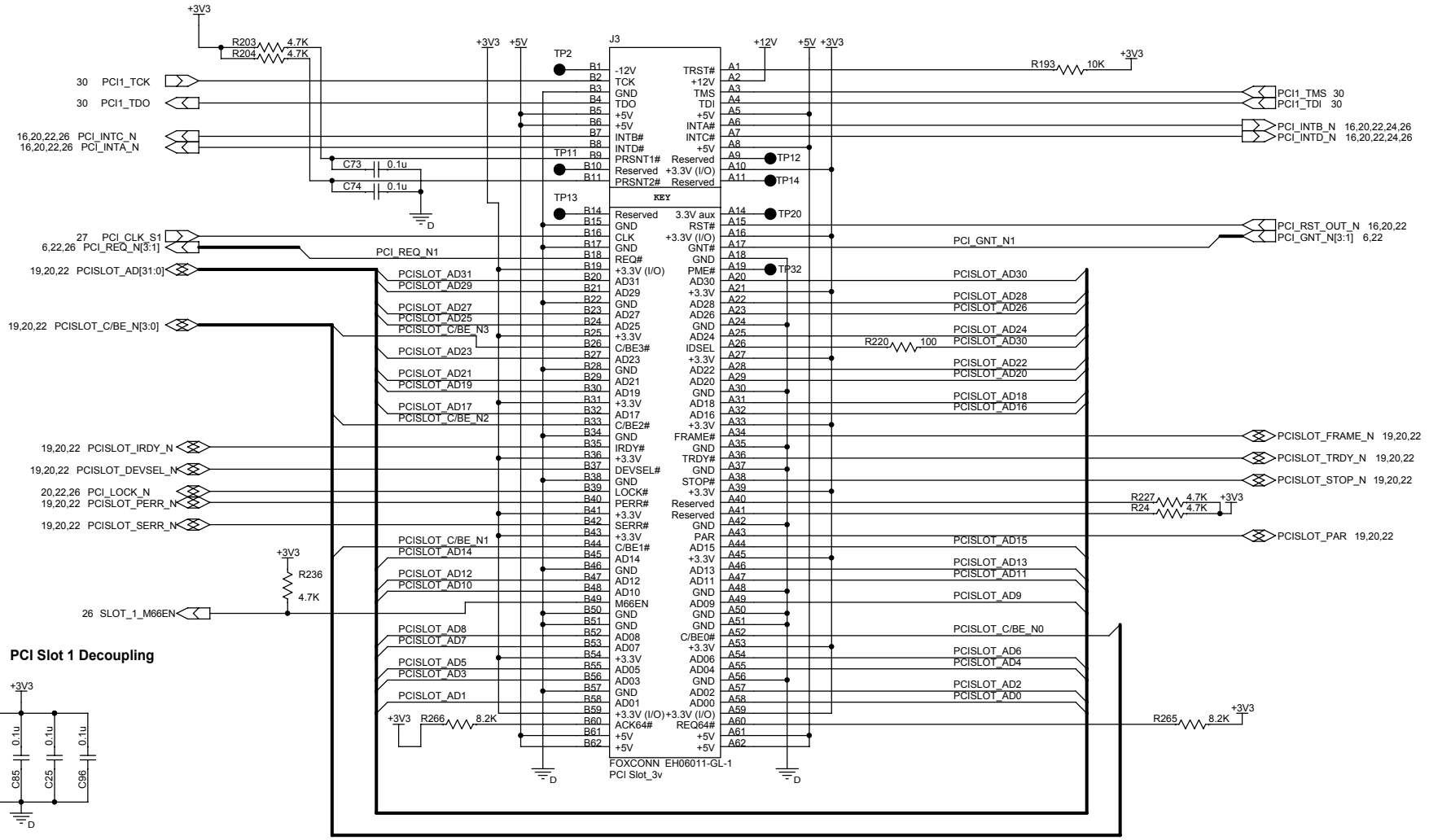
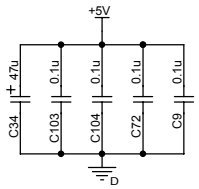
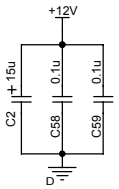


PCI Slot 1 Decoupling





If board is configured as a CPCI slot, none of the components on this page should be populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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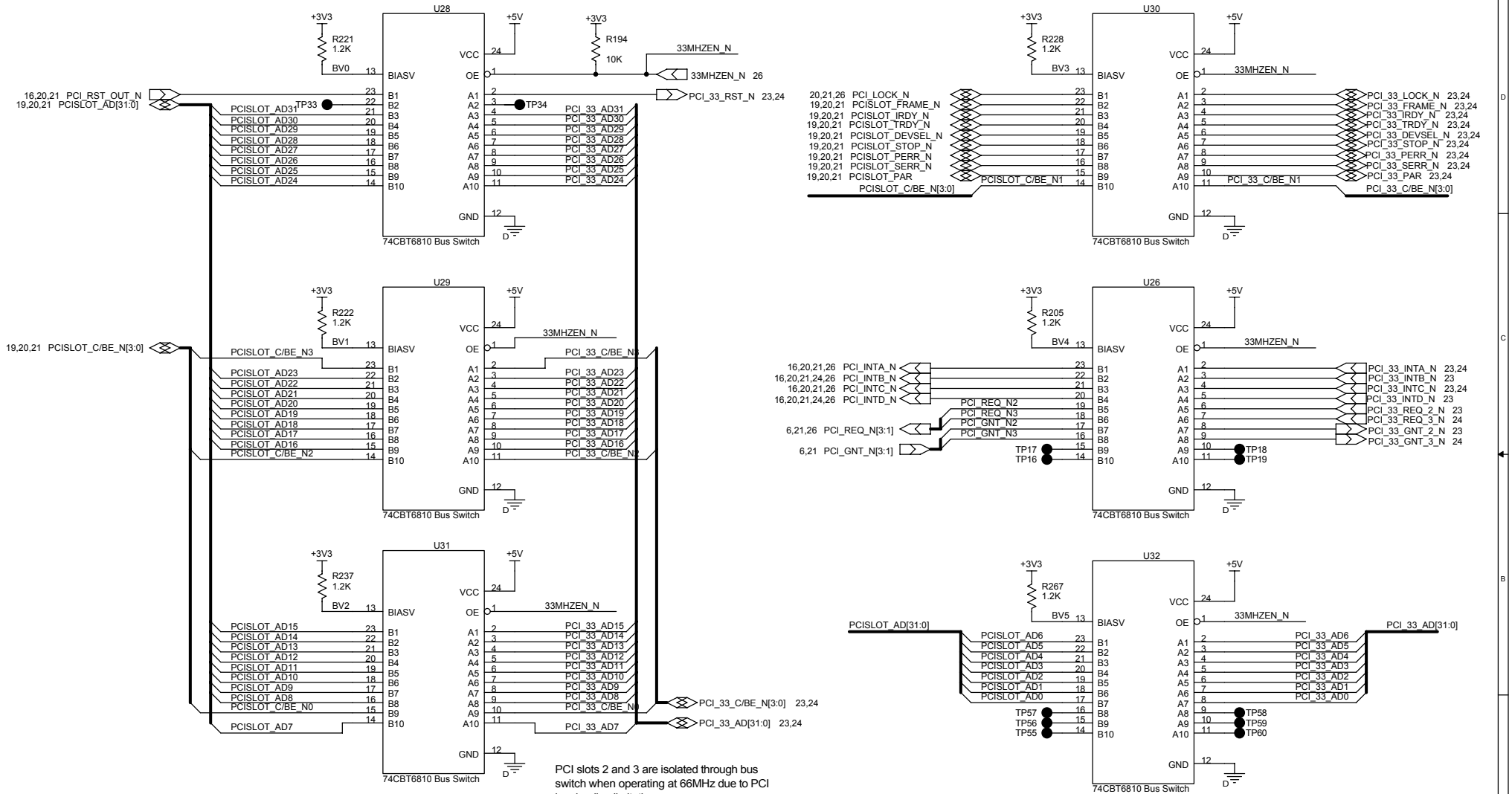
Title	**BIXMB425BD (REV A4) BASE CARD**	
Size: B	Page Title: PCI SLOT #1 (66 MHz capable)	Rev: 1.2
Date: Friday, October 03, 2003	Sheet 21 of 31	



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Title	BIXMB425BD (REV A4) BASE CARD	
Size B	Page Title: PCI Slot #2 - #3 Bus Switch	Rev 1.2
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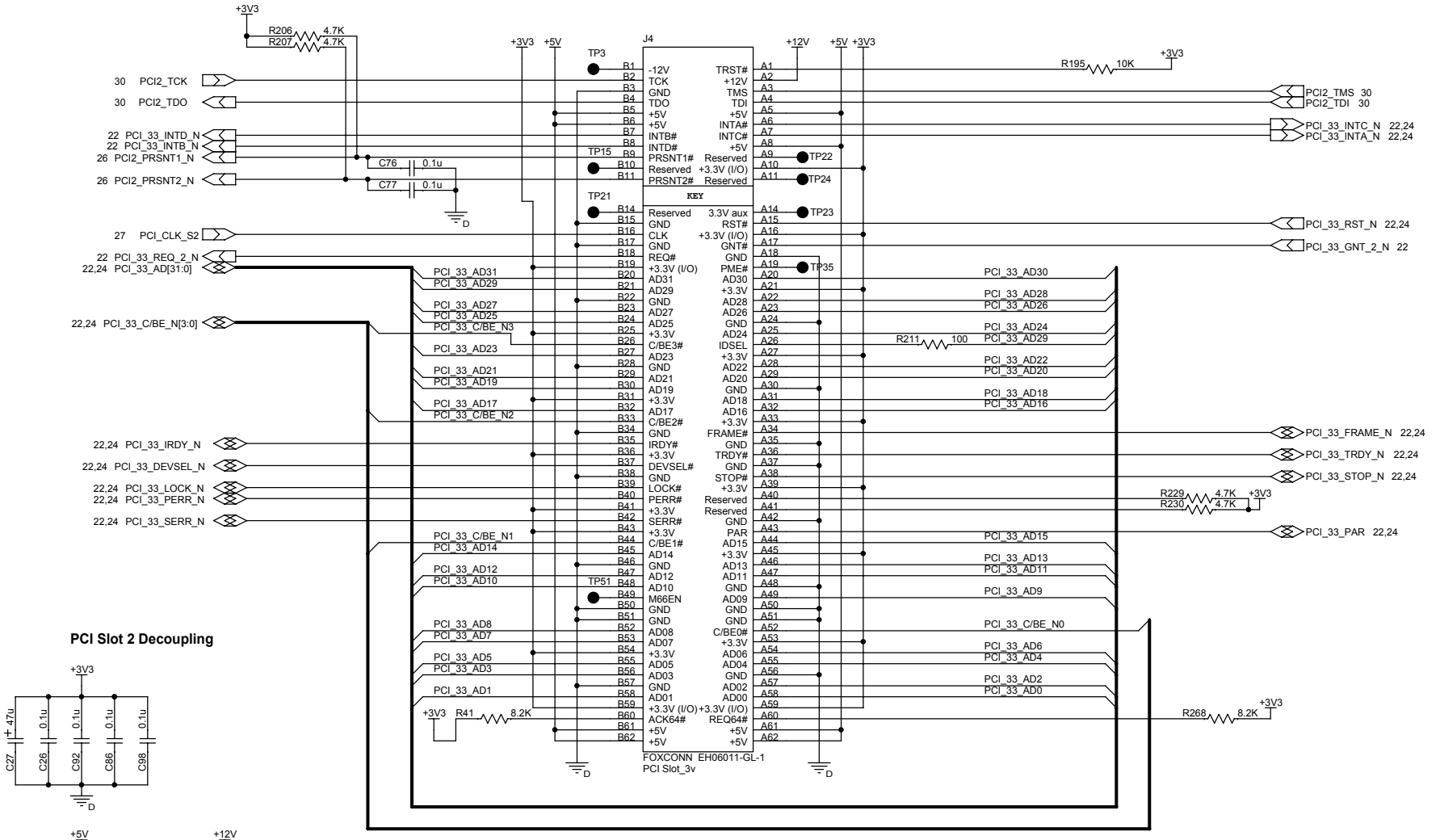

PCI Slot 2 Decoupling

If board is configured as a CPCI slot, none of the components on this page should be populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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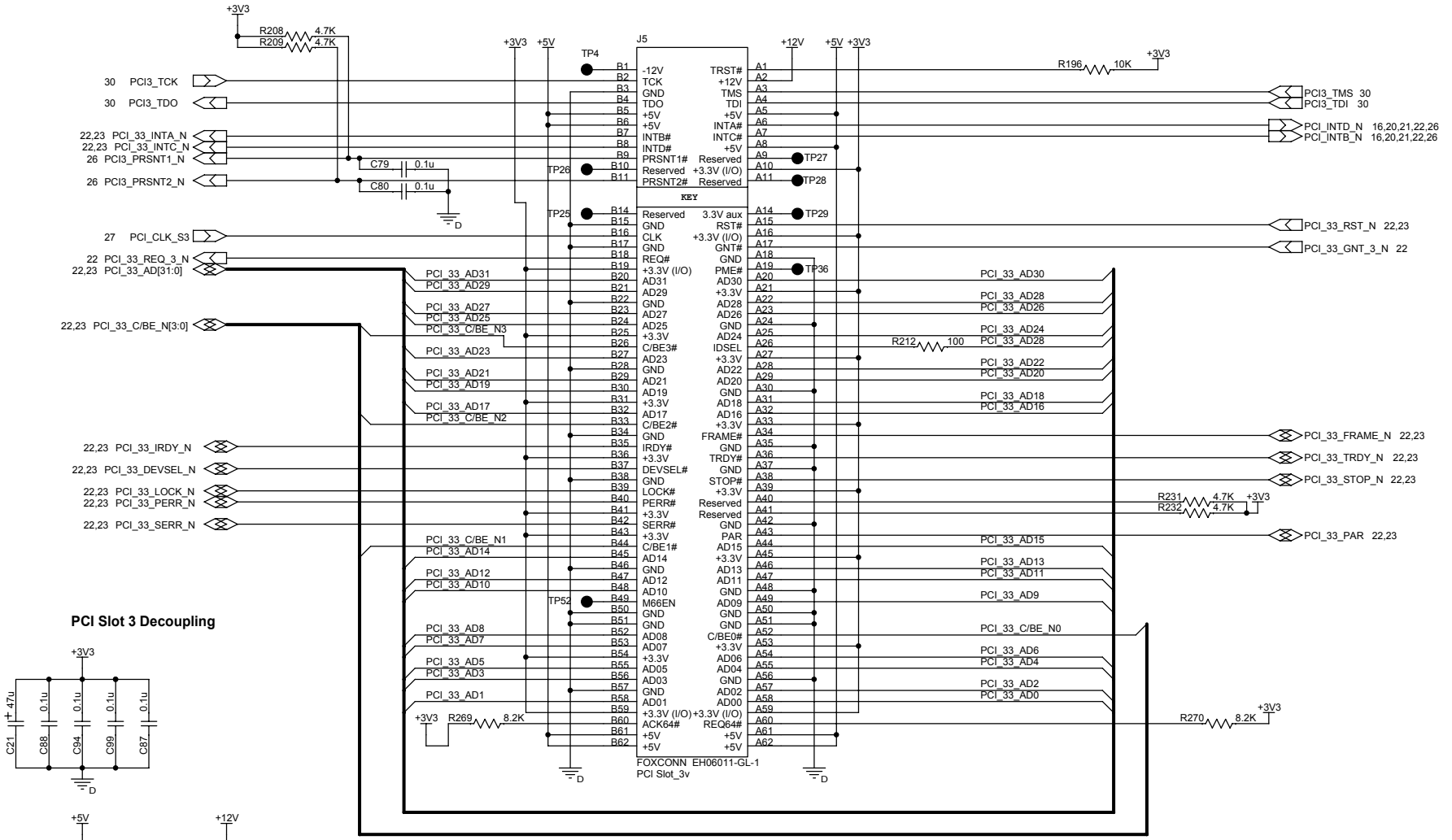
Title: **BIXMB425BD (REV A4) BASE CARD**	
Size: B — Page Title: PCI SLOT #2 (33 MHz only)	Rev: 1.2
Date: Friday, October 03, 2003 — Sheet 23 of 31	



If board is configured as a CPCI slot, none of the components on this page should be populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: PCI SLOT #3 (33 MHz only)	Rev 1.2
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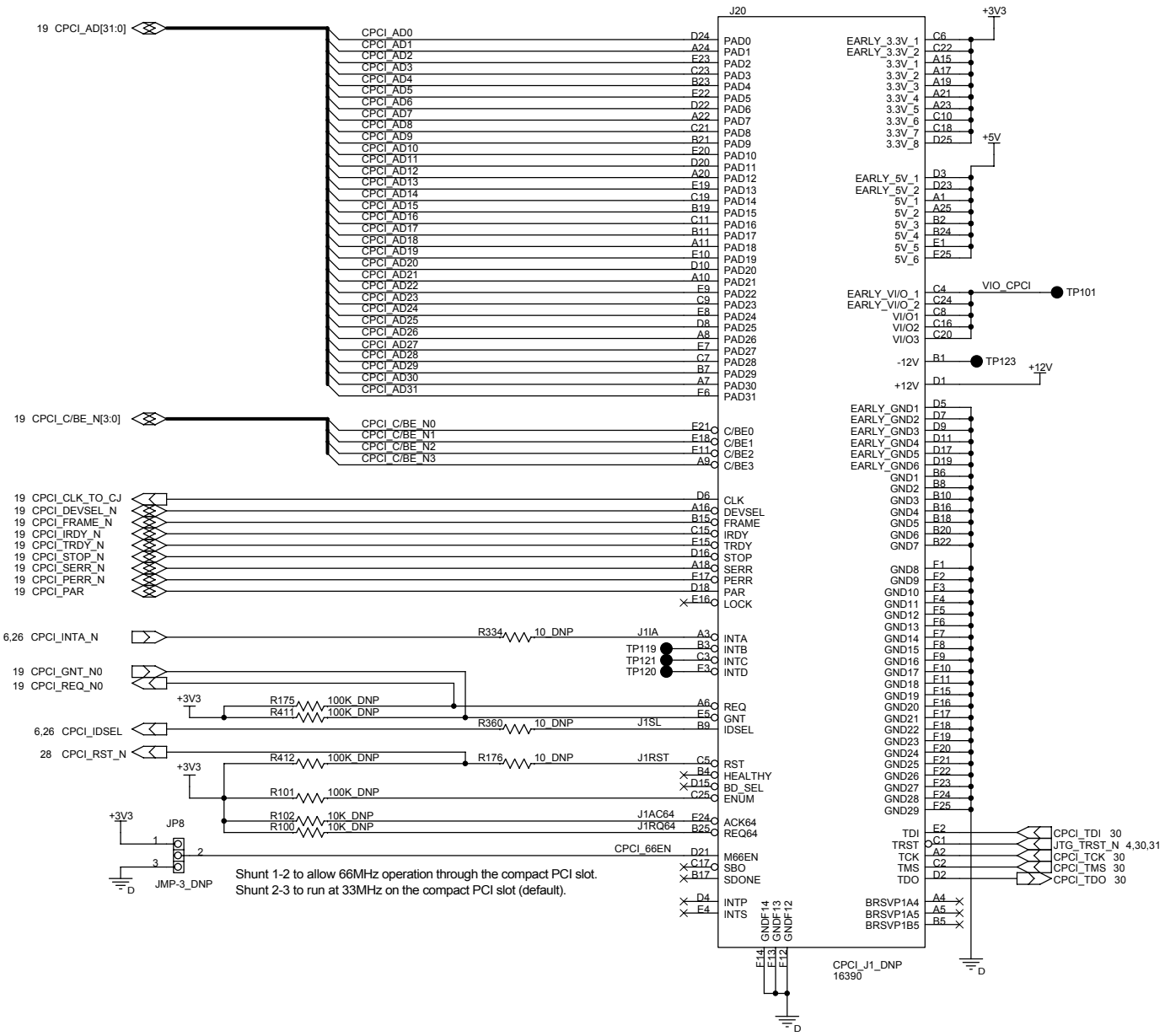

For a board configured as a PCI host, none of the components on this page should be populated. When the board is built as a CPCI slot, all components on this page are populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: cPCI Connector	Rev 1.2
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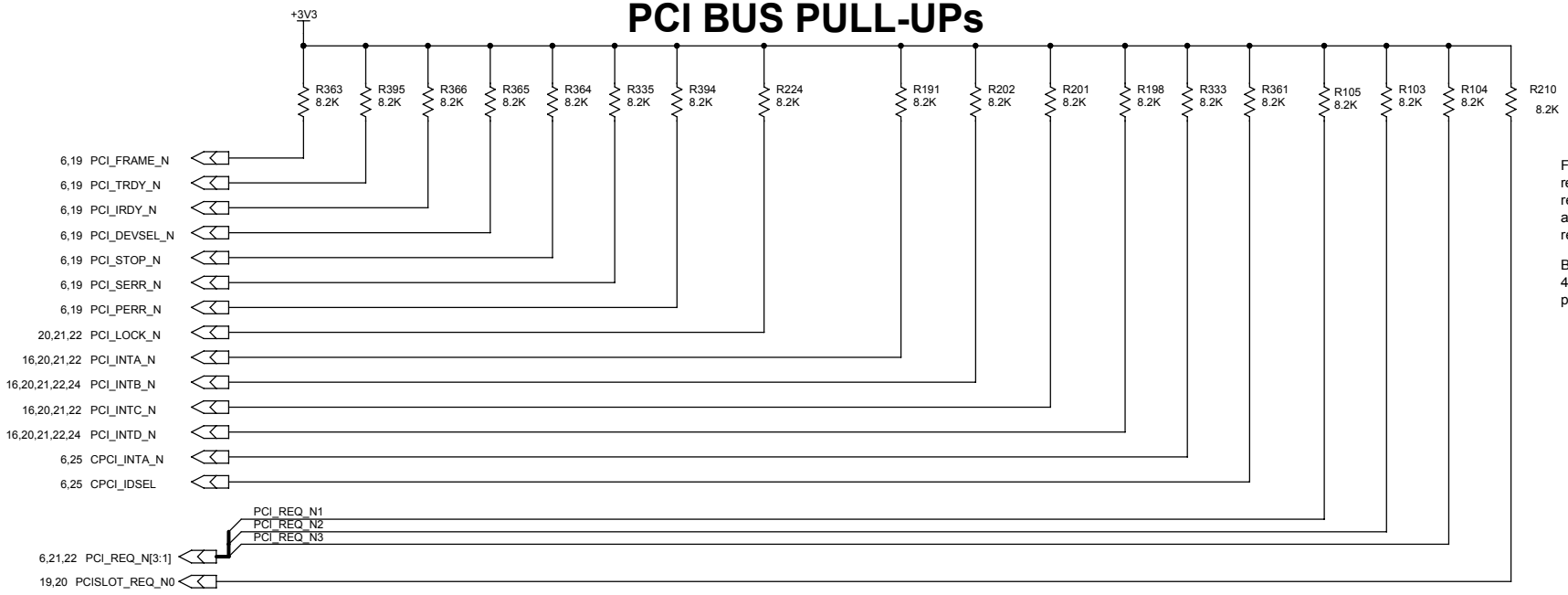
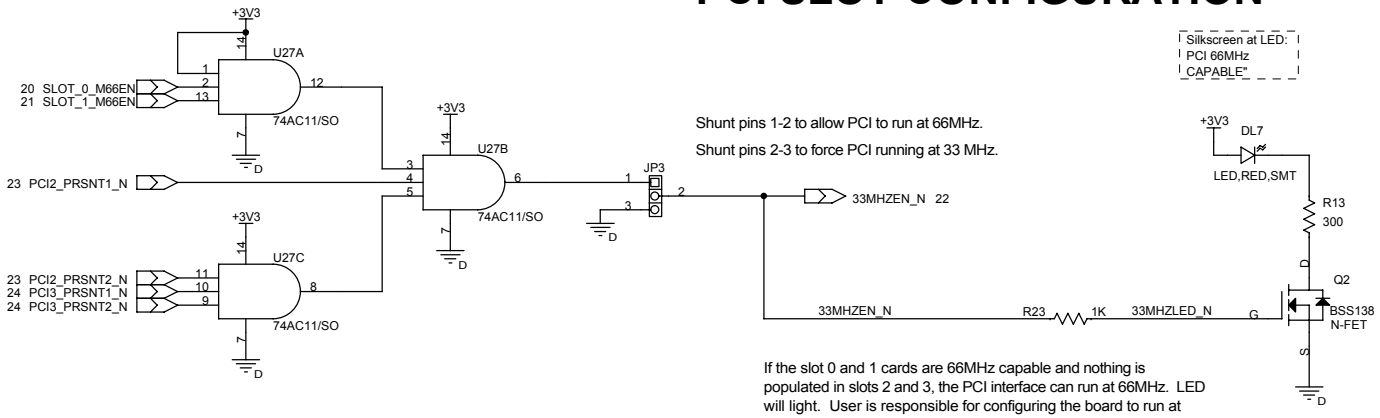
PCI BUS PULL-UPs



For customer designs, it is recommended that the 8.2K resistors shown on this page are replaced with 10K resistors.

Both reserved pins 40A and 41A are pulled up at each slot per PCI specification.

PCI SLOT CONFIGURATION



Shunt pins 1-2 to allow PCI to run at 66MHz.

Shunt pins 2-3 to force PCI running at 33 MHz.

If the slot 0 and 1 cards are 66MHz capable and nothing is populated in slots 2 and 3, the PCI interface can run at 66MHz. LED will light. User is responsible for configuring the board to run at 66MHz. EXPB_ADDR4 configuration strap and PCI clock header must be set correctly.

If board is configured as a CPCI slot, none of the components on this page should be populated.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	**BIXMB425BD (REV A4) BASE CARD**	
Size B	Page Title: PCI Pull-Ups and Configuration	Rev 1.2
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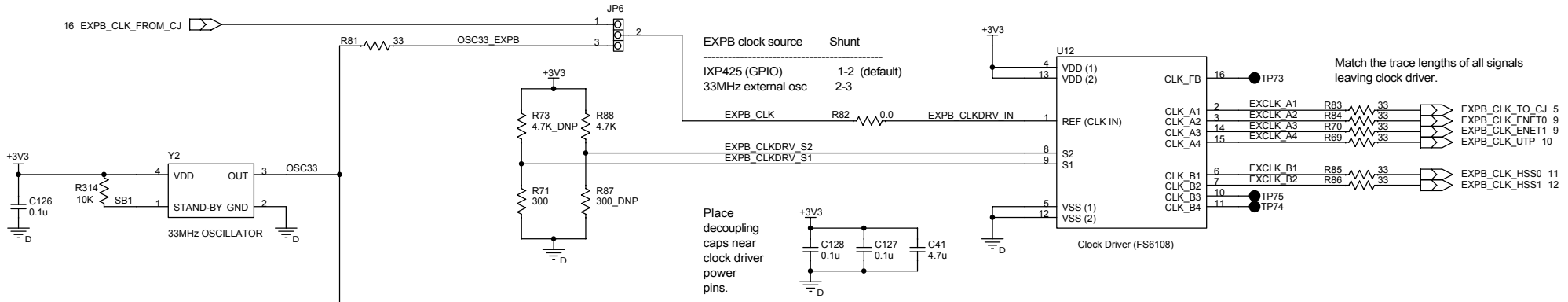
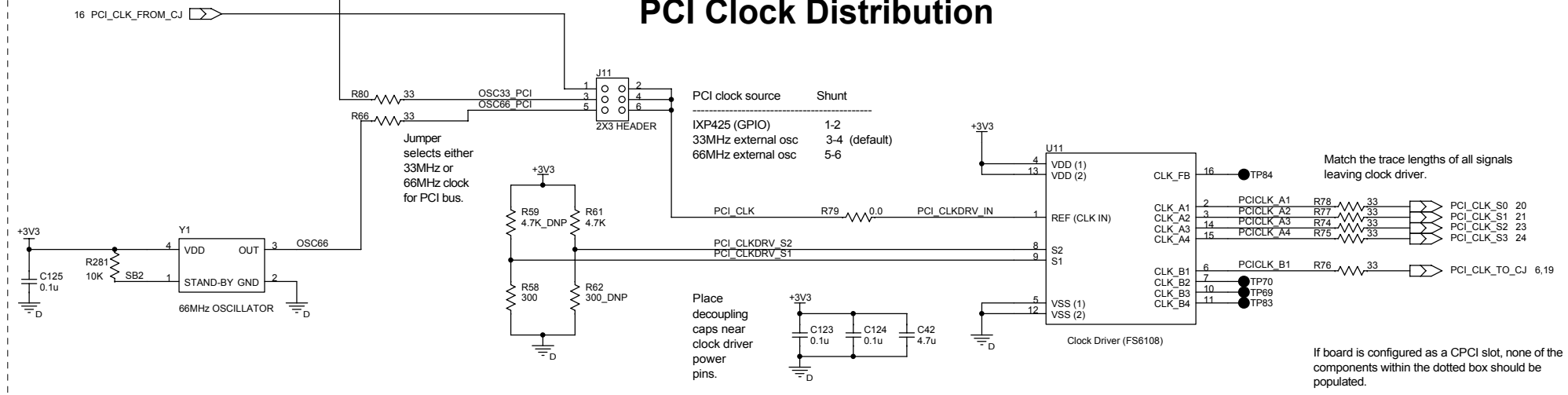
Expansion Bus Clock Distribution



PCI Clock Distribution



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
Size B	Page Title: PCI / Expansion Bus Clock Distribution	Rev 1.2
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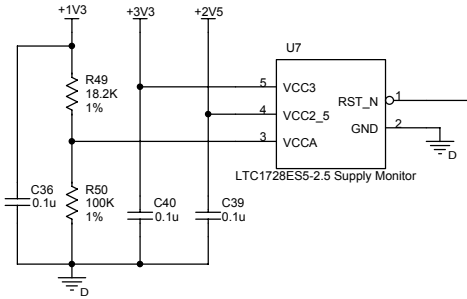
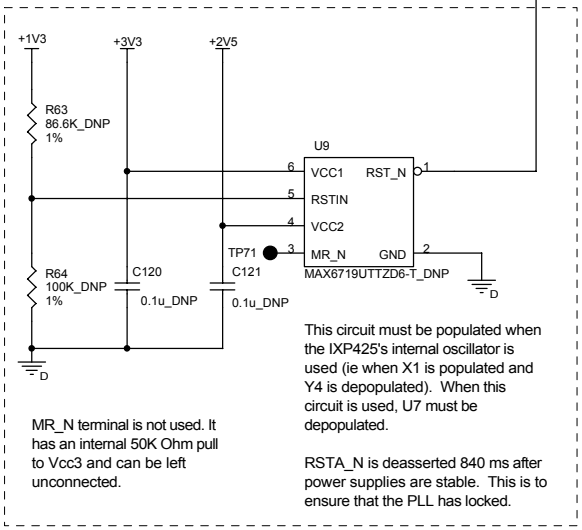
POWER GOOD / RESET CIRCUIT

The LTC1728 has an open drain output.
Reset will be asserted if voltages fall
below the following thresholds:
3.3V rail < 3.086V (typical)
2.5V rail < 2.338V (typical)
1.3V rail < 1.182V (typical)
Reset asserted for a minimum of 140ms.

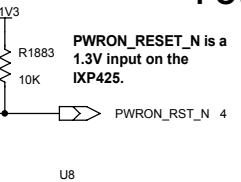




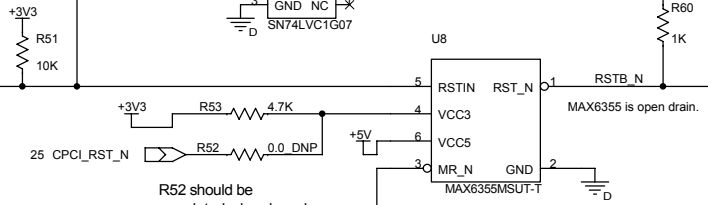
MR_N terminal is not used. It has an internal 50K Ohm pull to Vcc3 and can be left unconnected.

This circuit must be populated when the IXP425's internal oscillator is used (ie when X1 is populated and Y4 is depopulated). When this circuit is used, U7 must be depopulated.

RSTA_N is deasserted 840 ms after power supplies are stable. This is to ensure that the PLL has locked.

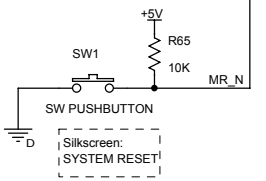


PWRON_RESET_N is a 1.3V input on the IXP425.

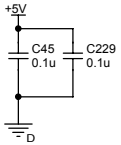


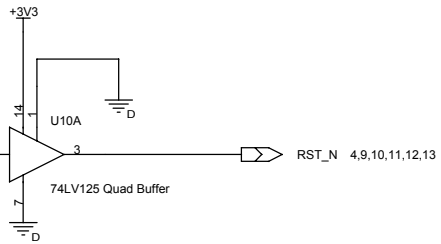
R52 should be populated when board is used as CPCI card. SW1 and R53 should be depopulated when board is used as a CPCI card.

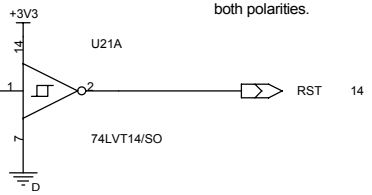
MAX6355 will assert reset for as long as SW_RST_N is asserted. Guaranteed minimum output pulse generated is 100 ms. Component provides debounce for pushbutton.



JTAG ICE port can generate a system reset.







Generate RESET in both polarities.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
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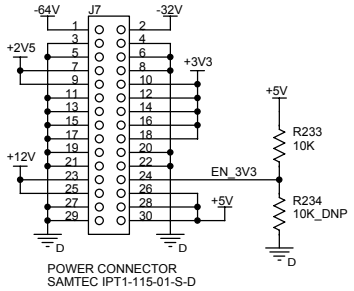
Power Module Connector



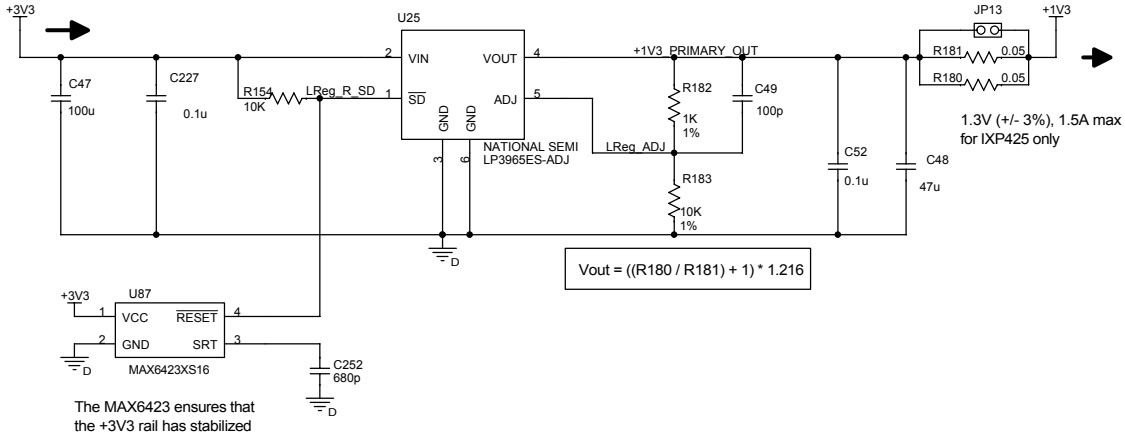
EN_3V3 enables +3V3 voltage regulation on the power module. When plugged used as a compactPCI card, this signal must be pulled low. Otherwise, it should be pulled high.

1.3V Regulator for IXP425 Core

Refer to the Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Datasheet for the power sequencing specification.

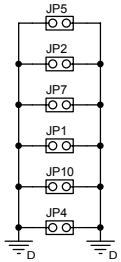
LAYOUT NOTE:
National Semiconductor recommends that the two resistors and cap off of pin 4 and 5 be as close as possible to the IC and have very short runs

IXP425 VCC Power Measurement:
Header placed for measurement purposes only. Choice of resistor divider feedback values and a effective sense resistance of 25 mOhm ensure IXP425 will receive 1.3V +/- 5%.



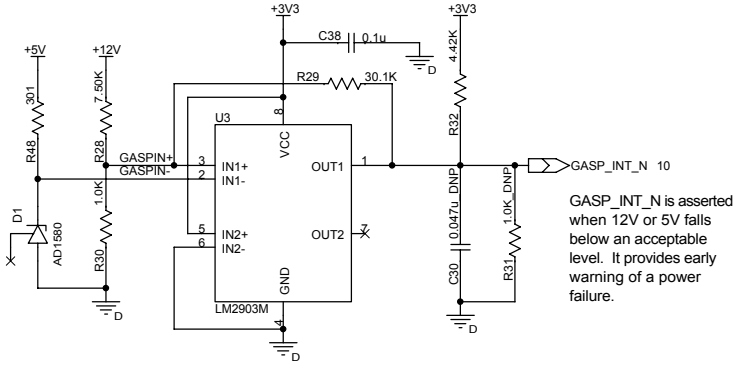
The MAX6423 ensures that the +3V3 rail has stabilized before +1V3 stabilizes. It has an open drain output.

Ground Headers



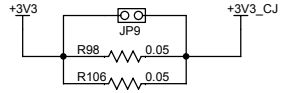
LAYOUT NOTE: Ground headers should be distributed on the board to provide easy ground points. Silkscreen should read "GND" on each header.

Gasp Circuit



GASP_INT_N is asserted when 12V or 5V falls below an acceptable level. It provides early warning of a power failure.

IXP425 VCCP Power Measurement



These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
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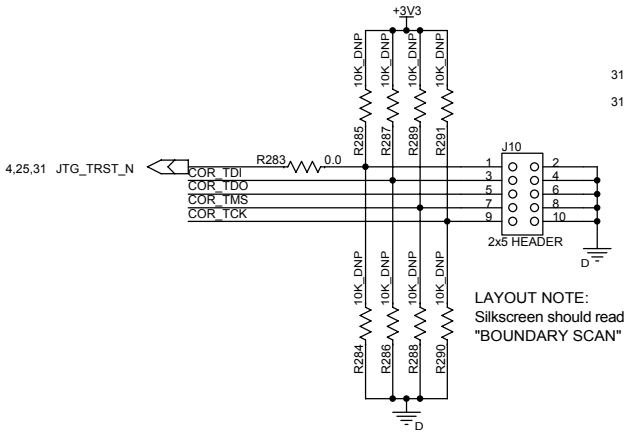
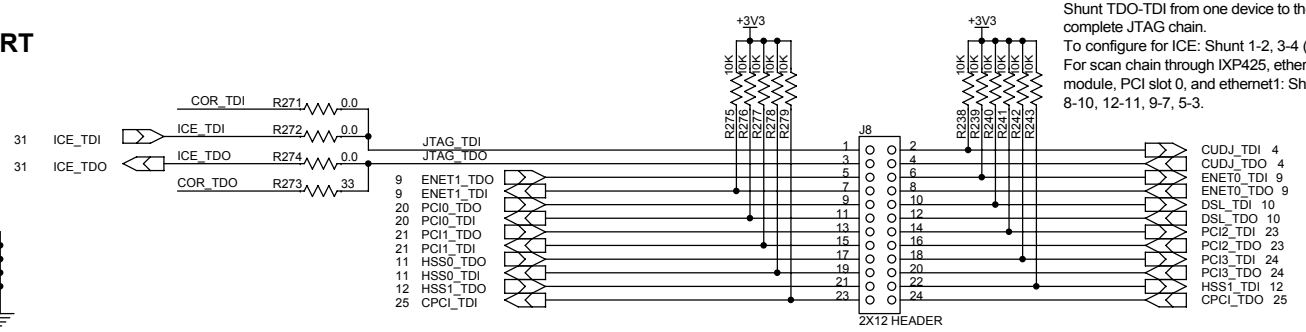
JTAG BOUNDARY SCAN TEST PORT



LAYOUT NOTE:
Silkscreen should read
"BOUNDARY SCAN"

TDI / TDO SELECTION HEADER

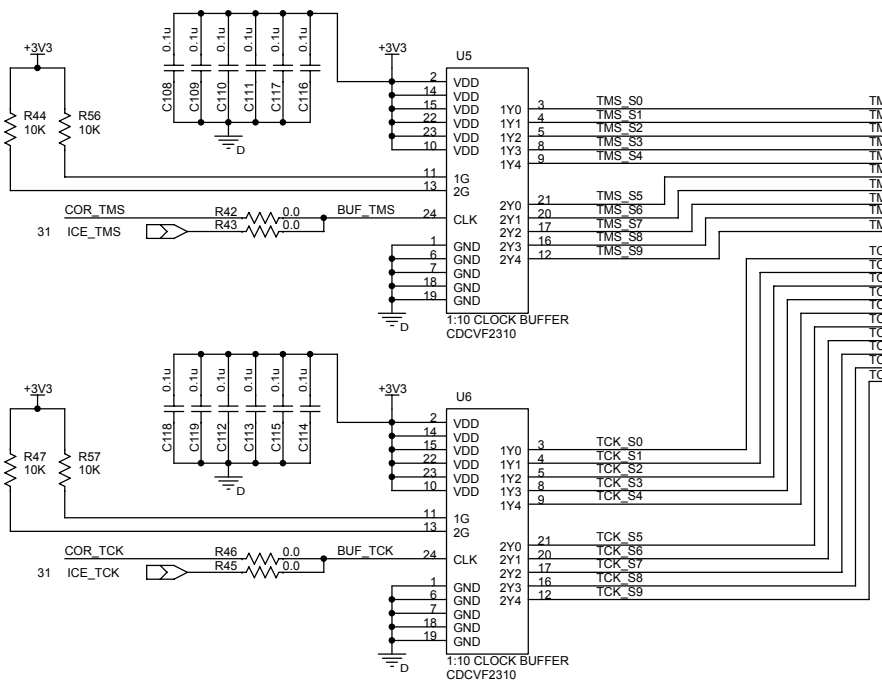


Shunt TDO-TDI from one device to the next to complete JTAG chain.
To configure for ICE: Shunt 1-2, 3-4 (default).
For scan chain through IXP425, ethernet0, DSL module, PCI slot 0, and ethernet1: Shunt 1-2, 4-6, 8-10, 12-11, 9-7, 5-3.

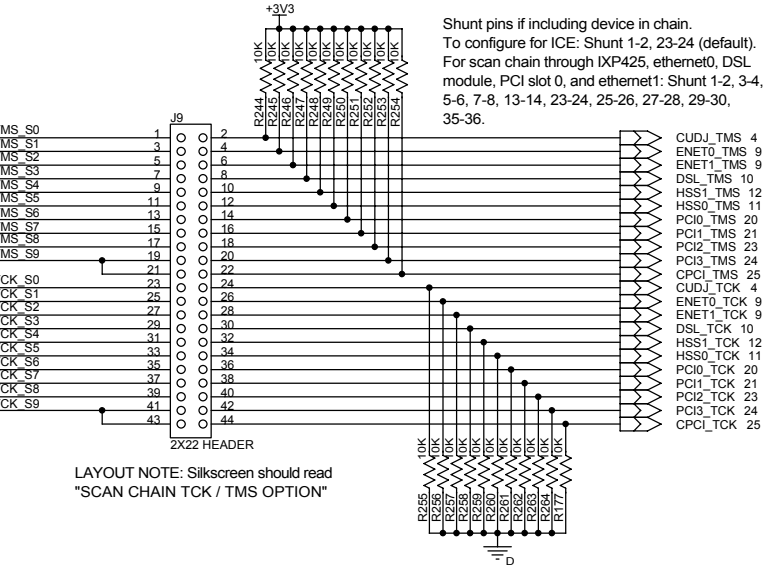
LAYOUT NOTE: Silkscreen should read
"SCAN CHAIN TDI / TDO OPTION"

TCK / TMS BUFFERS

25 ohm damping resistors built in to clock buffer.



TCK / TMS SELECTION HEADER



Shunt pins if including device in chain.
To configure for ICE: Shunt 1-2, 23-24 (default).
For scan chain through IXP425, ethernet0, DSL module, PCI slot 0, and ethernet1: Shunt 1-2, 3-4, 5-6, 7-8, 13-14, 23-24, 25-26, 27-28, 29-30, 35-36.

LAYOUT NOTE: Silkscreen should read
"SCAN CHAIN TCK / TMS OPTION"

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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Title	BIXMB425BD (REV A4) BASE CARD	
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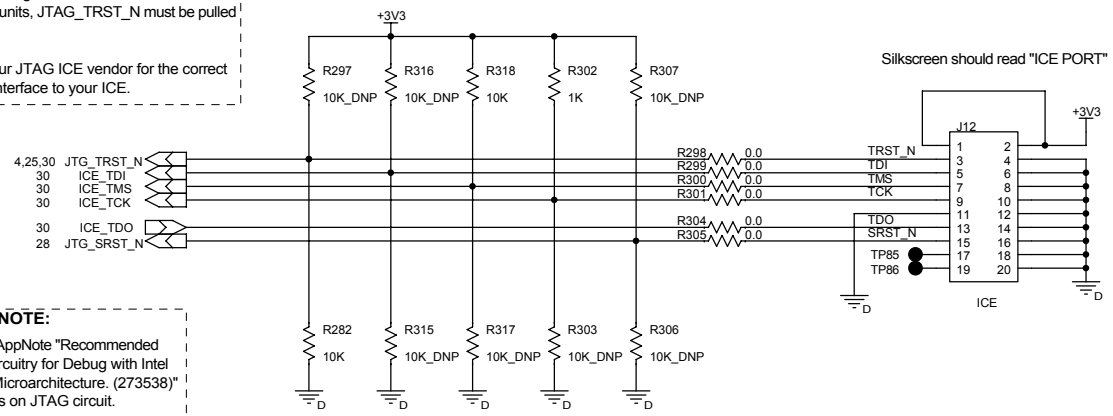
ICE JTAG Port

DESIGN NOTE:

For proper JTAG operation, JTG_TRST_N must be asserted at system power-on.

When not using the JTAG interface, such as in production units, JTAG_TRST_N must be pulled low.

Contact your JTAG ICE vendor for the correct ciruitry to interface to your ICE.



DESIGN NOTE:

See the AppNote "Recommended JTAG Circuitry for Debug with Intel Xscale Microarchitecture. (273538)" for details on JTAG circuit.

Unpopulated (DNP) resistor footprints placed to allow changes to JTAG circuitry as necessary.

These schematics should not be used as a reference design. Customers should consult the latest Intel IXP4XX datasheet for their design.

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