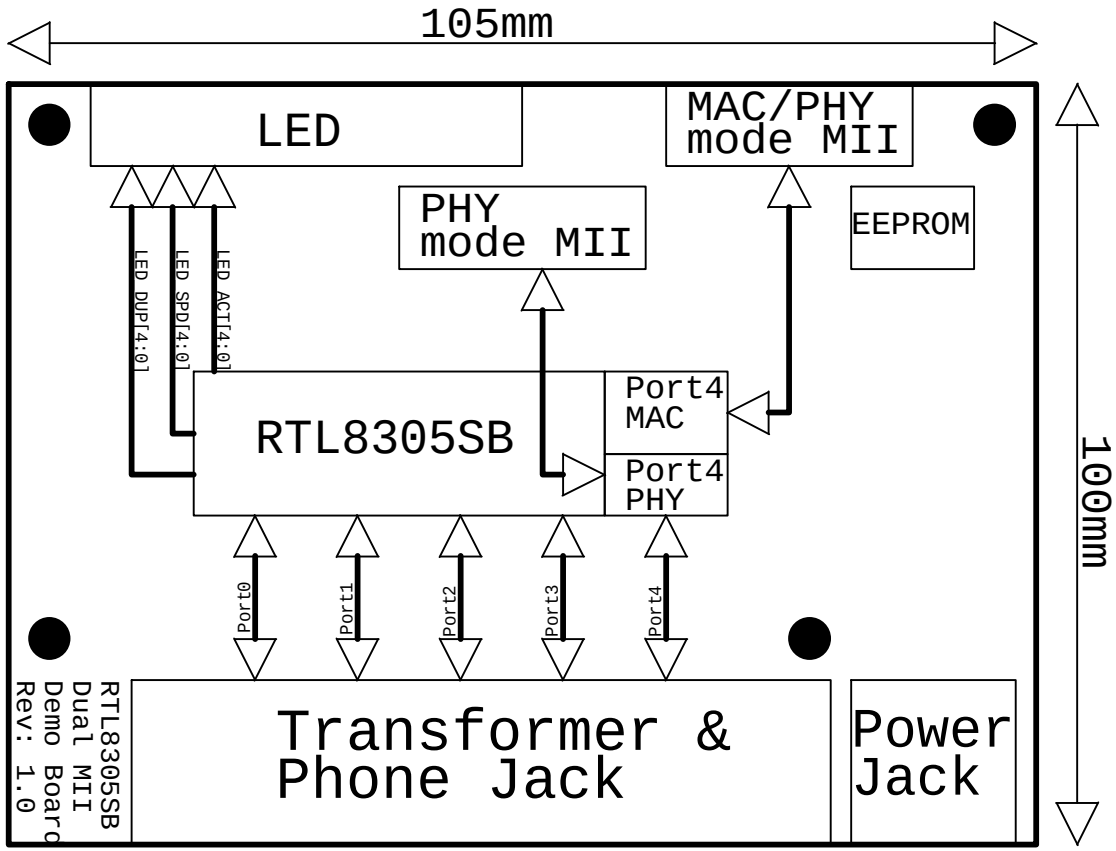
RTL8305SB Dual MII Demo Board



Component	RTL8305SB	RTL8305S
U3	Pulse H1102	Pulse H1102 or H1012
QXFRM1	Pulse H1164	Pulse H1062
C34, C35, C36, C37, C38	Assembly	Not Assembly
RS1, RS2, RS3, RS4, RS5	Not Assembly	Assembly
CS1, CS2, CS3, CS4, CS5	Not Assembly	Assembly
LS1, LS2	Not Assembly	Assembly
Q1	Assembly	Not Assembly
R72, R73	Assembly	Not Assembly

	Function For RTL8305SB
R3	Assembly to disable EEPROM Autoload
R4	Assembly to disable Half Duplex Backpressure Control
R5	Assembly to disable GroupX Full Duplex Flow Control
R6	Assembly to disable GroupX Full Duplex Flow Control
R8	Assembly to disable Auto Cross Over Function
R11	Change QoS Weighted Round Robin ratio
R13	Assembly to set Port3 as high priority port
R14	Assembly to enable VLAN tag priority
R15	Assembly to enable Broadcast Storm Control
R16	Assembly to enable VLAN function
RH1, RH3	Assembly to enable DEFER Control, RL1, RL3 should not assembly at the same time
RL1, RL3	Assembly to disable DEFER Control, RH1, RH3 should not assembly at the same time
RH2, RH4	Assembly to enable 48Pass1 Control, RL2, RL4 should not assembly at the same time
RL2, RL2	Assembly to disable 48Pass1 Control, RH2, RH4 should not assembly at the same time
J2/3, 4	Enable Dual MII Control, short with jumper to enable Dual MII function
J2/5, 6	Port 4 Link Status Control, short with jumper to force Port 4 link on
J2/7, 8	Port 4 Speed Control, open for 100Mbps and short for 10Mpbs
J2/9, 10	Port 4 Duplex Control, open for full duplex and short for half duplex
J2/11, 12	Port 4 Flow Control, open to enable and short to disable full duplex flow control
J2/13, 14, 15, 16	Port 4 Mode Control, [11]: UTP/MII MAC; [10]: 100Base-FX, [01]: MII PHY; [00]: SNI PHY

Note:

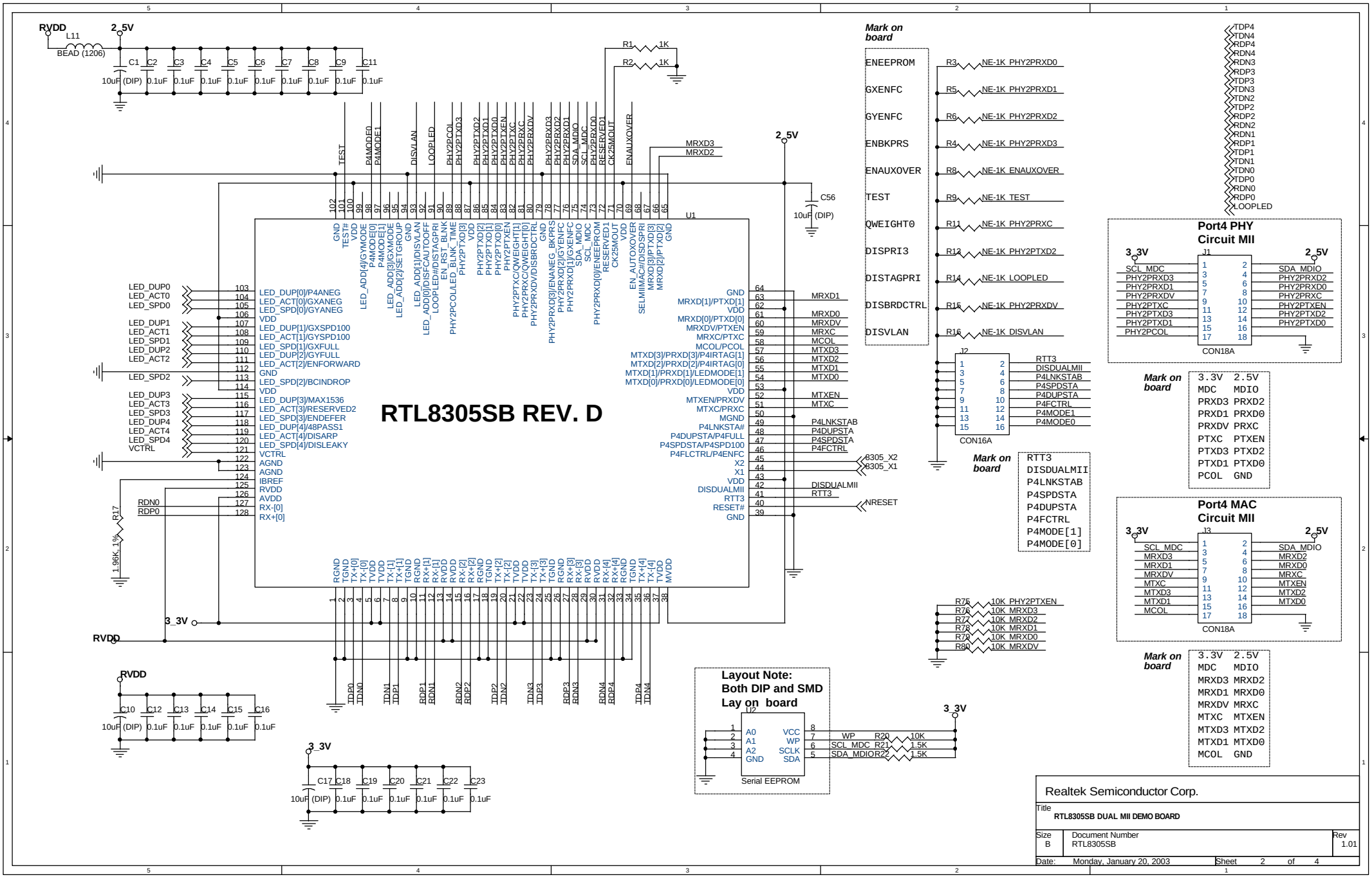
1: The demo board is 2 layer PCB and 1 side SMD for RTL8305SB, 2 side SMD for RTL8305S.
2: U2 should be 5V~2.5V power input capable, otherwise the VIN should be 3.3V.
3: RS1~RS5, CS1~CS5, LS1, LS2 are for RTL8305S and are placed on solder side.
4: Crystal shunt capacitor C52 and C53 should use 27pF.
5: For Defer, RH1 and RH3 are for ON, RL1 and RL3 are for OFF, should not coexist.
6: For 48Pass1, RH2 and RH4 are for ON, RL2 and RL4 are for OFF, should not coexist.
7: For LoopLED, R63 is for Loop indication and R14 is for tag priority enable, should not coexist.
8: R18 is for 3.3V and R19 is for 2.5V VIN capable EEPROM, should not coexist.
9: R1 and R2 are for EMI reduce test, optional for customers.
10: U3 could use H1102 or H1012 for RTL8305S, but only H1102 for RTL8305SB.
11: QXFRM1 should use H1062 for RTL8305S and H1164 for RTL8305SB.
12: L11 is used to seperate digital 2.5V and analog 2.5V power.
13: LS3-LS6 and L12-L15 are used for EMI test, optional for customers.
14: R17, IBREF resister should use 1.96K ohm.
15. J1 is Port 4 PHY circuit and J3 is Port 4 MAC circuit MII interface connectors.

Realtek Semiconductor Corp.

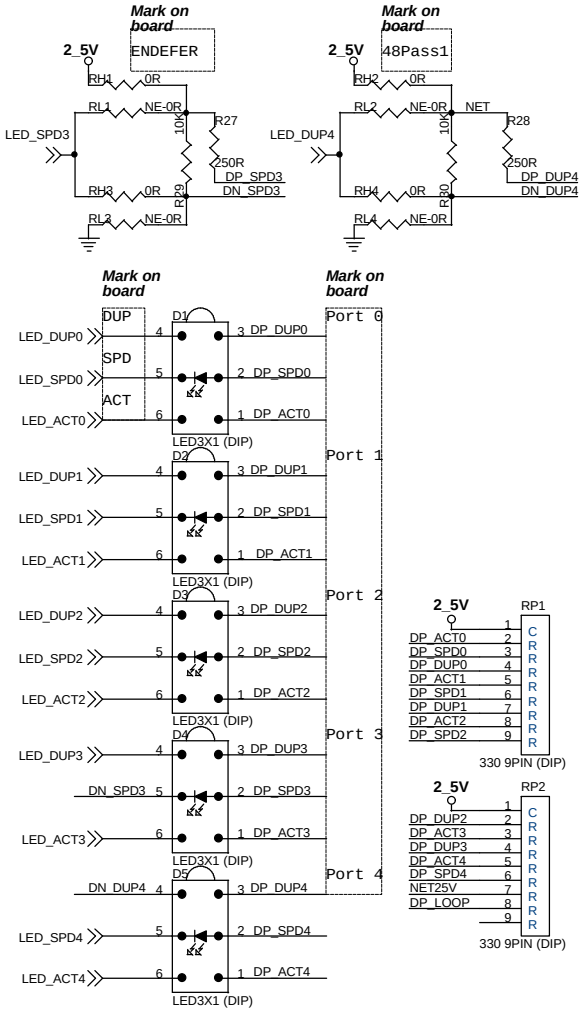
Title
RTL8305SB DUAL MII DEMO BOARD

Size	Document Number	Rev
A	BLOCK DIAGRAM	1.01

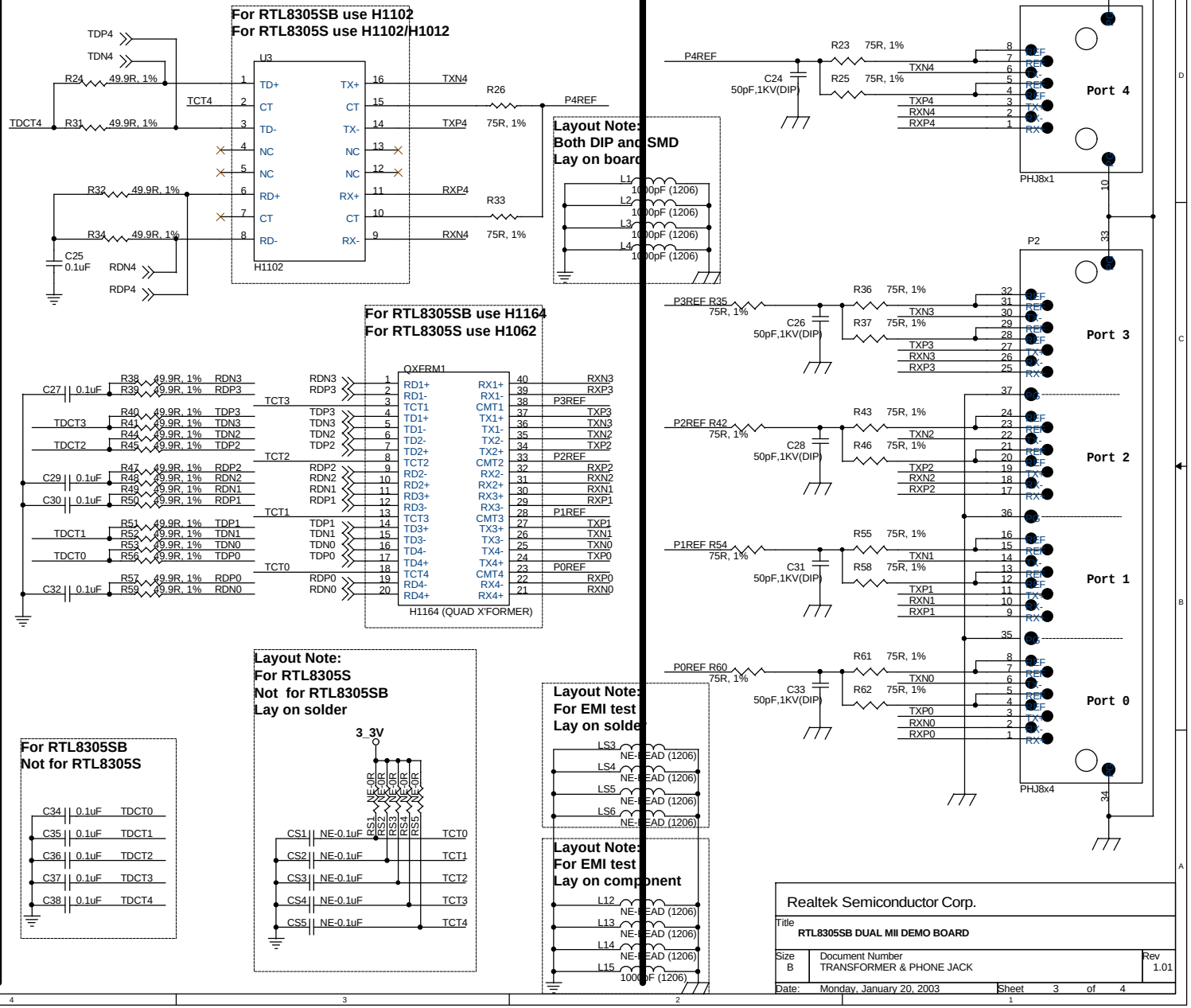
Date: Monday, January 20, 2003 Sheet 1 of 4


RTL8305SB REV. D
RVDD
2_5V
3_3V
L11
BEAD (1206)
U1
Mark on board
ENEEPROM
GXENFC
GYENFC
ENBKPRS
ENAUXOVER
TEST
QWEIGHT0
DISPRI3
DISTAGPRI
DISBRDCTRL
DISVLAN
Port4 PHY Circuit MII
Port4 MAC Circuit MII
CON18A
CON16A
Layout Note:
Both DIP and SMD
Lay on board
Serial EEPROM
Realtek Semiconductor Corp.
RTL8305SB DUAL MII DEMO BOARD
Document Number
RTL8305SB
Rev
1.01
Monday, January 20, 2003
Sheet 2 of 4

LED



TRANSFORMER



FRAME SIDE

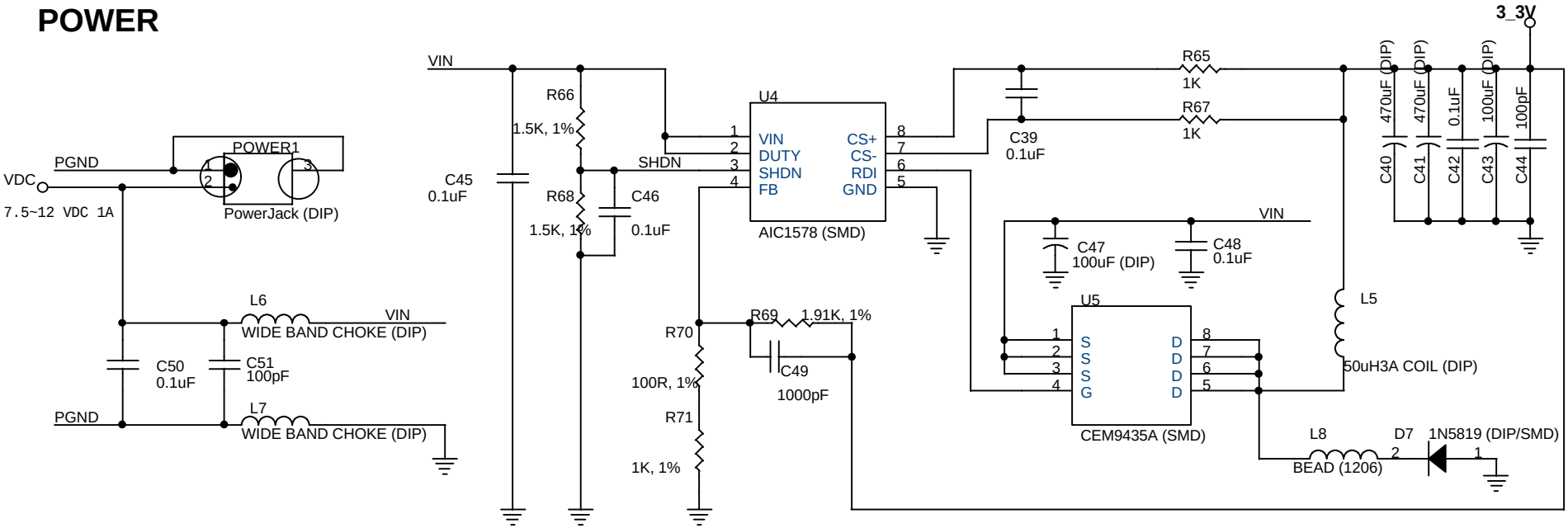
Realtek Semiconductor Corp.

Title: **RTL8305SB DUAL MII DEMO BOARD**

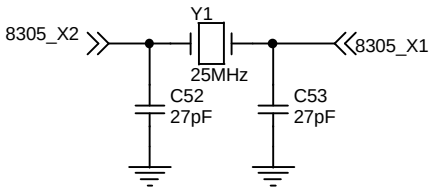
Size	Document Number	Rev
B	TRANSFORMER & PHONE JACK	1.01

Date: Monday, January 20, 2003 Sheet 3 of 4

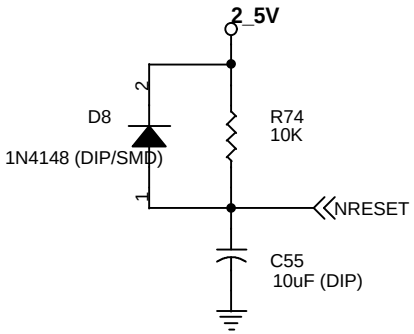
POWER



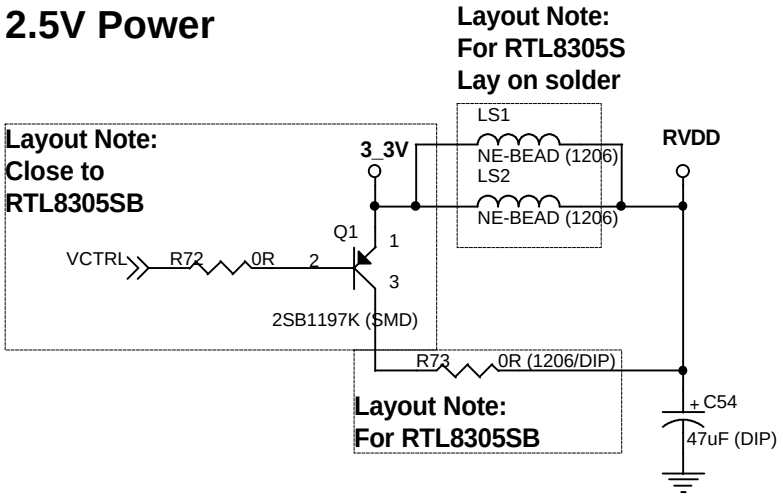
CLOCK

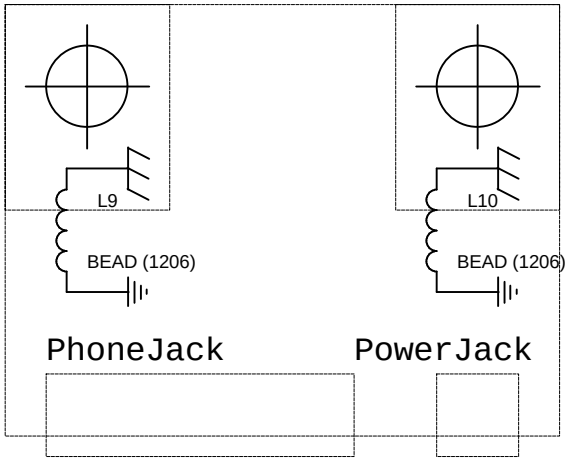


RESET



2.5V Power





Realtek Semiconductor Corp.		
Title: **RTL8305SB DUAL MII DEMO BOARD**		
Size: A	Document Number: POWER & CLOCK & RESET	Rev: 1.01
Date: Monday, January 20, 2003	Sheet 4 of 4	