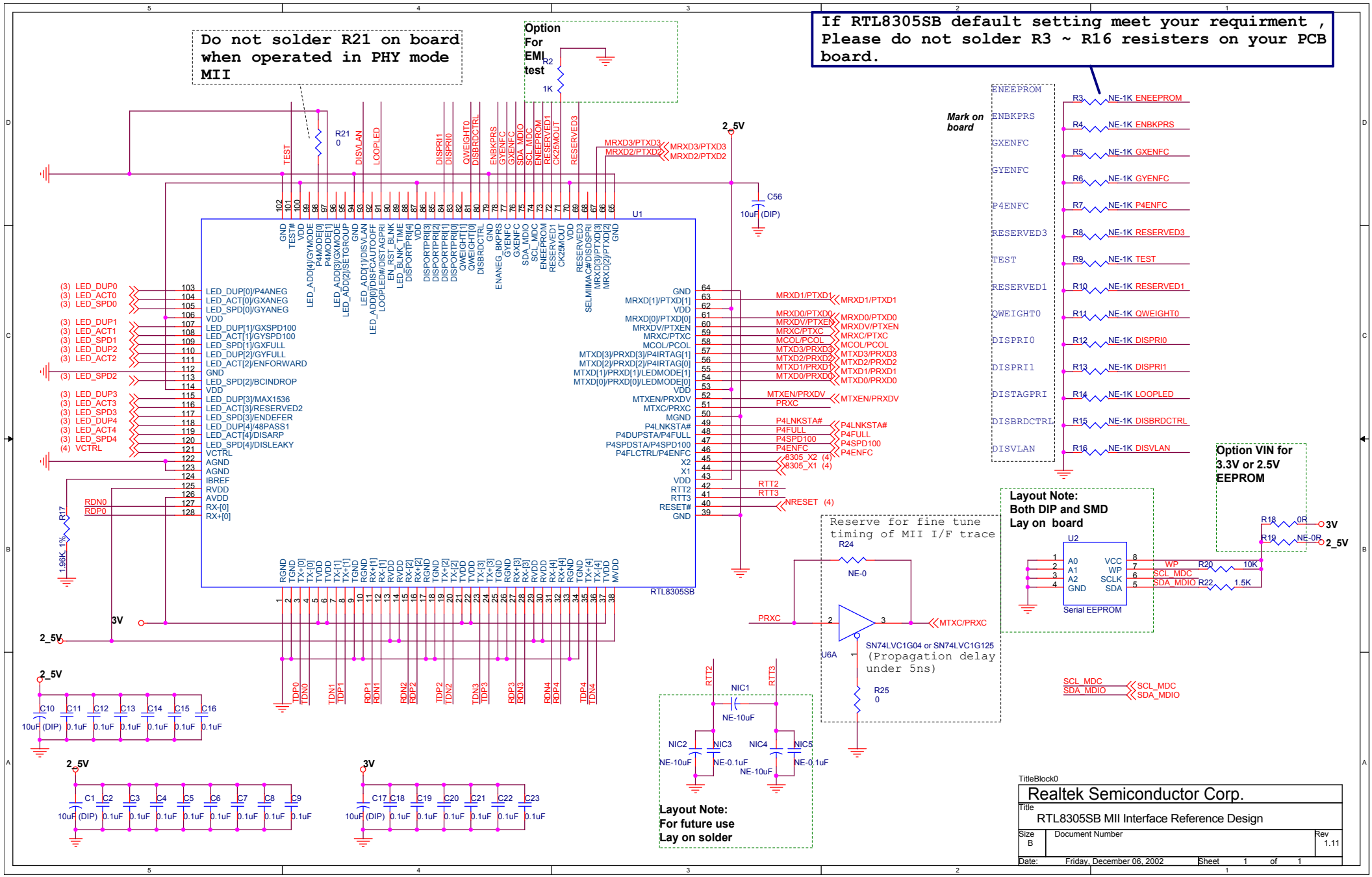
Do not solder R21 on board when operated in PHY mode MII
Option For EMI test
R2
1K
R21
0
If RTL8305SB default setting meet your requirment , Please do not solder R3 ~ R16 resisters on your PCB board.
Mark on board
ENEEPROM
ENBKPRS
GXENFC
GYENFC
P4ENFC
RESERVED3
TEST
RESERVED1
QWEIGHT0
DISPRI0
DISPRI1
DISTAGPRI
DISBRDCTRL
DISVLAN
R3 NE-1K ENEEPROM
R4 NE-1K ENBKPRS
R5 NE-1K GXENFC
R6 NE-1K GYENFC
R7 NE-1K P4ENFC
R8 NE-1K RESERVED3
R9 NE-1K TEST
R10 NE-1K RESERVED1
R11 NE-1K QWEIGHT0
R12 NE-1K DISPRI0
R13 NE-1K DISPRI1
R14 NE-1K LOOPLED
R15 NE-1K DISBRDCTRL
R16 NE-1K DISVLAN
2_5V
C56
10uF (DIP)
U1
RTL8305SB
MRXD3/PTXD3
MRXD2/PTXD2
MRXD1/PTXD1
MRXD0/PTXD0
MRXDV/PTXEN
MRXC/PTXC
MCOL/PCOL
MTXD3/PRXD3
MTXD2/PRXD2
MTXD1/PRXD1
MTXD0/PRXD0
MTXEN/PRXDV
PRXC
P4LNKSTA#
P4FULL
P4SPD100
P4ENFC
8305_X2 (4)
8305_X1 (4)
RTT2
RTT3
NRESET (4)
LED_DUP0
LED_ACT0
LED_SPD0
LED_DUP1
LED_ACT1
LED_SPD1
LED_DUP2
LED_ACT2
LED_SPD2
LED_DUP3
LED_ACT3
LED_SPD3
LED_DUP4
LED_ACT4
LED_SPD4
VCTRL
R17
1.96K 1%
RDN0
RDP0
3V
2_5V
Reserve for fine tune timing of MII I/F trace
R24
NE-0
PRXC
MTXC/PRXC
U6A
SN74LVC1G04 or SN74LVC1G125
(Propagation delay under 5ns)
R25
0
Layout Note:
Both DIP and SMD
Lay on board
U2
Serial EEPROM
WP
SCL_MDC
SDA_MDIO
R20 10K
R22 1.5K
Option VIN for 3.3V or 2.5V EEPROM
R18 0R
R19 NE-0R
3V
2_5V
SCL_MDC
SDA_MDIO
C10 C11 C12 C13 C14 C15 C16
10uF (DIP) 0.1uF
C1 C2 C3 C4 C5 C6 C7 C8 C9
C17 C18 C19 C20 C21 C22 C23
NIC1 NE-10uF
NIC2 NE-10uF
NIC3 NE-0.1uF
NIC4 NE-10uF
NIC5 NE-0.1uF
Layout Note:
For future use
Lay on solder
TitleBlock0
Realtek Semiconductor Corp.
Title
RTL8305SB MII Interface Reference Design
Size B
Document Number
Rev 1.11
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Note:

RTL8305SB			Connect to CPU pins	
PIN NAME	**PIN#**	**TYPE**	**SNI mode (MPC850)**	**MII mode**
MTXC/PRXC	51	O	**RXC (RCLK)**	**RXC**
MTXEN/PRXDV	52	O	**RXDV&CRS (CD)**	**RXDV&CRS**
MTXD0/PRXD0	54	O	**RXD (RXD)**	**RXD0**
MTXD1/PRXD1	55	O	floating	**RXD1**
MTXD2/PRXD2	56	O	floating	**RXD2**
MTXD3/PRXD3	57	O	floating	**RXD3**
MCOL/PCOL	58	O	**COL (CTS)**	**COL**
MRXC/PTXC	59	O	**TXC (TCLK)**	**TXC**
MRXDV/PTXEN	60	I	**TXEN (RTS)**	**TXEN**
MRX0/PTXD0	61	I	**TXD (TXD)**	**TXD0**
MRXD1/PTXD1	63	I	floating	**TXD1**
MRXD2/PTXD2	66	I	floating	**TXD2**
MRXD3/PTXD3	67	I	floating	**TXD3**
P4MODE[0]	98	I	strapped low	floating
P4LNKSTA#	49	I		LOW FOR LINK_ON
P4FULL	48	I		Floating OR Pull up FOR FULL DUPLEX
P4SPD100	47	I		Floating or Pull up FOR 100M
P4ENFC	46	I		Floating or Pull up FOR FLOW CONTROL ON

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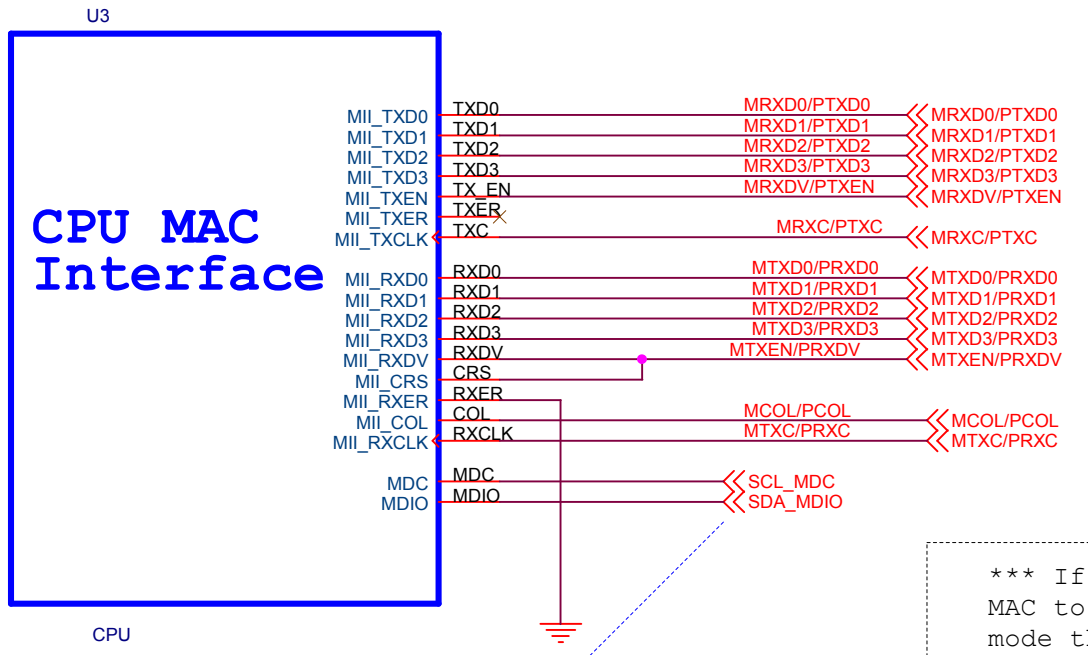

*** If you force the CPU MAC to operated in force mode then the MDC/MDIO are not used.

*** The MII signals trace length should not longer than 10 cm and trace width should great than 10 mil atleast.

Note:

RTL8305SB's port 4 MII Interface PHY address = 4, and register of port 4 only the register bit 1.2(Link Status) , 0.13(Spd_Sel) , 0.8(Duplex Mode) could be read by Serial management Interface (MDC/MDIO).

Realtek Semiconductor Corp.		
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