Genesys Logic, Inc.

GL880S

PCI USB 2.0
UHCI And EHCI Host Controller

Datasheet
Revision 1.00
Jul. 15, 2004

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Office:

Genesys Logic, Inc.
12F, No. 205, Sec. 3, Beishin Rd., Shindian City,
Taipei, Taiwan
Tel: (886-2) 8913-1888
Fax: (886-2) 6629-6168

http://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	07/15/2004	First formal release

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

The GL880S is a PCI-based USB 2.0 Host Controller. It integrates 1 Universal Host Controller (for full-speed/low-speed transactions) and 1 Enhanced Host Controller (for high-speed transactions). It provides higher bandwidth (480 Mbps) and is backward compatible with USB 1.1.

The GL880S supports 2 downstream facing ports with 1.5 (low-speed), 12 (full-speed) and 480 (high-speed) Mbps transaction capability. This chip also supports PCI-Bus Power Management Interface Specification 1.1 and provides legacy support for all downstream facing ports. The GL880S is ready to provide a PCI 2-port USB2.0 peripheral-interface for every segment of desktop and mobile computers. Support for the GL880S is built into Microsoft Windows XP and Windows 2000.

CHAPTER 2 FEATURES

- Complies with Universal Serial Bus Specification rev. 2.0.
- Complies with Universal Host Controller Interface Design Guide rev. 1.1.
- Complies with Enhanced Host Controller Interface Specification rev. 1.00.
- Complies with 32-bit, 33 MHz PCI Local Bus Specification Interface rev. 2.3.
- Complies with PCI Power Management Interface Specification rev. 1.1 for power reduction mode.
- Supports configurable number of downstream ports (2).
- Integrates high-speed/ full-speed/ low-speed transceivers in all downstream ports.
- Supports two color LED indicators for each USB port.
- Legacy support for keyboard and mouse.
- 12MHz external clock to provide better EMI.
- 3.3V power supply.
- PCI pads with 3.3V-driving, 5V-tolerant.
- Above 2.5 kV ESD protection.
- 0.35 μm process.
- Available in 128-pin LQFP package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

Figure 3.1 - Pinout Diagram

3.2 Pin List

Table 3.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	VDD	P	33	AD11	I/O	65	NC	-	97	PLLVDD	P
2	GND	P	34	AD10	I/O	66	NC	-	98	PLLGND	P
3	CBEJ3	I/O	35	AD9	I/O	67	NC	-	99	OSCX1	I
4	IDSEL	I	36	AD8	I/O	68	NC	-	100	OSCX2	O
5	AD23	I/O	37	CBEJ0	I/O	69	TESTM	I	101	OSCVDD	P
6	AD22	I/O	38	AD7	I/O	70	NC	-	102	OSCGND	P
7	AD21	I/O	39	VDD	P	71	PIN_EN	I	103	NC	-
8	AD20	I/O	40	GND	P	72	PWRENJ1	O	104	NC	-
9	AD19	I/O	41	AD6	I/O	73	OCJ1	I	105	NC	-
10	VDD	P	42	AD5	I/O	74	PWRENJ2	O	106	NC	-
11	GND	P	43	AD4	I/O	75	OCJ2	I	107	AVDD2	P
12	AD18	I/O	44	AD3	I/O	76	VDDAUX	P	108	AGND2	P
13	AD17	I/O	45	AD2	I/O	77	GND	P	109	NC	-
14	AD16	I/O	46	AD1	I/O	78	NC	-	110	NC	-
15	CBEJ2	I/O	47	VDD	P	79	NC	-	111	NC	-
16	FRAMEJ	I/O	48	GND	P	80	NC	-	112	NC	-
17	IRDYJ	I/O	49	AD0	I/O	81	NC	-	113	VDD	P
18	TRDYJ	I/O	50	CRUNJ	I/O	82	PRSTJ	I	114	GND	P
19	DEVSELJ	I/O	51	SMIJ	O	83	PMEJ	O	115	INTJ	O
20	VDD	P	52	PROMEN	O	84	VDDAUX	P	116	PCICLK	I
21	GND	P	53	PROMDO	I	85	GND	P	117	GNTJ	I
22	STOPJ	I/O	54	PROMCS	O	86	DMF1	I/O	118	REQJ	O
23	NC	-	55	PROMDI	O	87	DMH1	I/O	119	AD31	I/O
24	NC	-	56	VDD	P	88	DPH1	I/O	120	AD30	I/O
25	PAR	I/O	57	GND	P	89	DPF1	I/O	121	VDD	P
26	CBEJ1	I/O	58	PROMSK	O	90	AVDD1	P	122	GND	P
27	AD15	I/O	59	AIND1	O	91	AGND1	P	123	AD29	I/O
28	AD14	I/O	60	GIND1	O	92	DMF2	I/O	124	AD28	I/O
29	AD13	I/O	61	AIND2	O	93	DMH2	I/O	125	AD27	I/O
30	VDD	P	62	GIND2	O	94	DPH2	I/O	126	AD26	I/O
31	GND	P	63	NC	-	95	DPF2	I/O	127	AD25	I/O
32	AD12	I/O	64	NC	-	96	RREF	I/O	128	AD24	I/O

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

PCI Interface			
Pin Name	**Pin#**	**Type**	**Description**
PRSTJ	82	I (pd)	PCI reset
PCICLK	116	I	PCI system clock (33 MHz)
REQJ	118	O (pd)	PCI request
GNTJ	117	I (pd)	PCI grant (tri-state)
AD[31:0]	119,120, 123~128, 5~9,12~14, 27~29, 32~36,38, 41~46,49	I/O	PCI address and data
PAR	25	I/O	PCI parity
CBEJ[3:0]	3,15,26, 37	I/O (pd)	PCI command and byte enables
FRAMEJ	16	I/O (pd)	PCI cycle frame
IRDYJ	17	I/O (pd)	PCI initiator ready
TRDYJ	18	I/O (pd)	PCI target ready
STOPJ	22	I/O (pd)	PCI stop
IDSEL	4	I	PCI initialization device select
DEVSELJ	19	I/O (pd)	PCI device select
INTJ	115	O (pd)	PCI interrupt signal for UHCI host controller1 (open drain)
PMEJ	83	O (pd)	PCI power management event (open drain)
CRUNJ	50	I/O (pd)	PCI clock control (open drain)

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
OCJ[1:2]	73,75	I (pd)	Over-current detect input
PWRENJ[1:2]	72,74	O (pd)	Port power enable
DPF[1:2]	89,95	I/O	D+ for full/low speed operation
DMF[1:2]	86,92	I/O	D- for full/low speed operation
DPH [1:2]	88,94	I/O	D+ for high speed operation
DMH [1:2]	87,93	I/O	D- for high speed operation
GIND[1:2]	60,62	O	Green LED output for port indicator (open drain)
AIND[1:2]	59,61	O	Amber LED output for port indicator (open drain)

System Interface			
Pin Name	**Pin#**	**Type**	**Description**
OSCX1	99	I	Crystal input (12 MHz)
OSCX2	100	O	Crystal output (12 MHz)
RREF	96	I/O	510Ωreference resistor
SMIJ	51	O	System management interrupt for legacy support
TESTM	69	I (pu)	Test mode 0: enter test mode; 1: normal operation

EEPROM Interface			
Pin Name	**Pin#**	**Type**	**Description**
PROMEN	52	O	EEPROM Chip enable
PROMDO	53	I	EEPROM Chip data in
PROMCS	54	O	EEPROM Chip select
PROMDI	55	O	EEPROM Chip data out
PROMSK	58	O	EEPROM Chip clock

Other Interface			
Pin Name	**Pin#**	**Type**	**Description**
NC	65,66	-	No connection
PIN_EN	71	-	Pull up 10KΩ resistor

Power / Ground			
Pin Name	**Pin#**	**Type**	**Description**
VDD	1,10,20,30, 39,47,56, 113,121	P	Power for digital logic part
GND	2,11,21,31, 40,48,57, 77,85,114, 122	P	Ground for digital logic part
AVDD	90,107	P	Power for USB transceiver part
AGND	91,108	P	Ground for USB transceiver part
PLLVDD	97	P	Power for internal PLL
PLLGND	98	P	Ground for internal PLL
VDDAUX	76,84	P	3.3V auxiliary power
OSCVDD	101	P	Power for internal OSC
OSCGND	102	P	Ground for internal OSC

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 REGISTERS

This section lists the PCI configuration registers and operational registers for UHCI0/UHCI1/EHCI.

4.1 PCI Configuration Registers Descriptions

4.1.1 Function 0/1 Universal Host Controller Interface

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Device ID	0x02h	15:0	RO	0x8083h	Genesys Logic UHCI's device ID
Vendor ID	0x00h	15:0	RO	0x17A0h	Genesys Logic's Vendor ID
Command	0x04h	15:10	RO	000000b	Reserved
		9	RO	0b	GL880S doesnot supprt Fast Back-to-Back cycle.
		8	R/W	0b	SERRJ Enable: This bit is an enable bit for the SERRJ driver. 0: Disables the SERRJ driver 1: Enables the SERRJ driver
		7	RO	0b	Reserved
		6	R/W	0b	Parity Error Response: This bit controls the device's response to parity errors. 0: The device sets its Detected Parity Error status bit(bit15 in the Status register) when an error is detected, but does not assert PERRJ and continues normal operation 1: The device must take its normal action when a parity error is detected. GL880S will not assert PERRJ when this bit = 1.
		5	RO	0b	GL880S does not support palette snoop cycles.
		4	RO	0b	GL880S does not support Memory Write and Invalidate Command
		3	RO	0b	GL880S does not support Special Cycles.
		2	R/W	0b	Bus Master: Controls a device's ability to act as a master on the PCI bus. 0: Disables the device from generating PCI accesses. 1: Allows the device to behave as a bus master.
		1	RO	0b	UHCI0 does not support memory access.
		0	R/W	0b	I/O Space Enable: Controls a device' s response to I/O space accesses. 0: disables 1: enable
Status	0x06h	15	R/W1C	0b	Detected Parity Error: This bit is set by GL880S whenever it detects a parity error even if parity error handling is disabled.
		14	R/W1C	0b	Signaled System Error: This bit is set whenever GL880S detected SERRJ event, but will not assert SERRJ signal.

		13	R/W1C	0b	Received Master Abort: This bit is set by GL880S whenever its transaction is terminated with Master-Abort.
		12	R/W1C	0b	Received Target Abort: This bit is set by GL880S whenever its transaction is terminated with Target-Abort.
		11	R/W1C	0b	Signaled Target Abort: This bit is set by GL880S whenever it terminates a transaction with Target-Abort.
		10:9	RO	01b	DEVSEL timing: GL880S support medium decode.
		8	R/W1C	0b	Master Data Parity Error: This bit is only implemented by bus masters. It is set when three conditions are met: (1) The bus agent asserted PERRJ itself (on a read) or observed PERRJ asserted(on a write); (2) The agent setting the bit acted as the bus master for the operation in which the error occurred; (3) The Parity Error Response bit (Command and register) is set.
		7	RO	0b	Fast Back-to-Back Capable: Fast Back-to –Back is not supported.
		6	RO	0b	Reserved
		5	RO	0b	GL880S does not support 66MHz operation.
		4	RO	1b	Capability List: GL880S implement Power Management capability.
		3:0	RO	0000b	Reserved
Class Code	0x09h	23:16	RO	0ch	BaseClass: Serial Bus Controller Device
		15:8	RO	03h	SubClass USB Device
		7:0	RO	00h	Interface Universal Host Controller
Revision ID	0x08h	7:0	RO	00h	Version 0.0
BIST	0x0fh	7:0	RO	00h	BIST is not supported
Header Type	0x0eh	7:0	RO	80h	PCI Multi-function device
Latency Timer	0x0dh	7:0	R/W	00h	Latency Timer for this PCI bus master
Cache Line Size	0x0ch	7:0	R/W	00h	Cache Line Size
Base Address Register	0x10h	31:16	RO	0000h	Reserved
		15:5	R/W	000h	Corresponds to I/O address signals AD[15:5] respectively.
		4:1	RO	0000b	Reserved
		0	RO	1b	Base address register field in this register maps to I/O space.
Subsystem ID	0x2eh	15:0	RO	0000h	Indicates Subsystem ID
Subsystem Vender ID	0x2ch	15:0	RO	0000h	Indicates Subsystem Vender ID

Capability Pointer	0x34h	7:0	RO	40h	Power Management Capability List header
Max_Lat	0x3fh	7:0	RO	00h	Frequency request of PCI access
Min_Gnt	0x3eh	7:0	RO	00h	Minimum request for burst period
Interrupt Pin	0x3dh	7:0	RO	01h	Routing to INTAJ
Interrupt Line	0x3ch	7:0	R/W	ffh	Indicates interrupt line's route
PMC	0x42h	15	RO	0b	Indicates whether D3cold is supported or not.
		14:11	RO	1111b	PMEJ can be asserted from D0,D1,D2,D3hot.
		10	RO	1b	D2_Support: Support D2 Power Management State
		9	RO	1b	D1_Suport: Support D1 Power Management State
		8:6	RO	00b	Aux_Current Indicates current requirement If PMEJ generation from D3cold is not supported by this host controller core, this field must return a value of "000b" when read. If PMEJ generation from D3cold is supported by this host controller core, following assignments apply: Bit Vaux 8 7 6 Max.CurrentRequired 1 1 1 375mA 1 1 0 320mA 1 0 1 270mA 1 0 0 220mA 0 1 1 169mA 0 1 0 100mA 0 0 1 55mA 0 0 0 0mA
		5	RO	0b	Does not required Specific Initialization before the generic class device driver is able to use it.
		4	RO	0b	Reserved
		3	RO	0b	PME Clock: PCICLK is not required for PMEJ assertion
		2:0	RO	010b	Version: PCI Power Management Interface Specification release 1.1
Next Pointer	0x41h	7:0	RO	00h	No next item in the list
Capability ID	0x40h	7:0	RO	01h	PCI Power Management Interface
PMCSR	0x44h	15	R/W1C	0b	PME_Status: This bit is set to "1" when the function would normally assert PMEJ sugnal independent of the state of the PME_En bit. Writing a "1" to this bit will clear it and cause the function to stop asserting a PMEJ (if enabled). Writing a "0" has no effect.
		14:13	RO	00b	Data_Scale: Data register is not implemented.
		12:9	RO	0000b	Data_Select: Data register is not implemented.

		8	R/W	0b	PME_En: Enable to assert PMEJ. 0b: PMEJ assertion disable 1b: PMEJ assertion enable This bit defaults to "0" if the host controller core does not support PMEJ generation from D3cold. If the host controller core supports PMEJ generation from D3cold, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.
		7:2	RO	00h	Reserved
		1:0	R/W	00b	Power State: To shows power state of a host controller core and sets the host controller core into a new power state. 00b: D0 01b: D1 10b: D2 11b: D3hot
SBRN	0x60h	7:0	RO	10h	Serial Bus Specification Release Number 1.0
UHCI Legacy Support	0xC0h-0xC1h (UHCI0 only)	15	R/W1C	0	SMI Caused by End of Pass-through. Indicates whether the event occurred. 1: Event Occurred 0: Software clears this bit by writing a 1 to the bit location.
		14	RO	0	Reserved
		13	R/W	1	PCI Interrupt Enable. Used to prevent the USB controller from generating an interrupt due to transactions on its ports. 1: Enable 0: Disable
		12	RO	0	SMI Caused by USB Interrupt. Indicates whether the event occurred. 1: Event Occurred 0: No event occurred.
		11	R/W1C	0	SMI Caused by Port 64 Write. Indicates whether the event occurred. 1: Event Occurred 0: Software clears this bit by writing a 1 to the bit location.
		10	R/W1C	0	SMI Caused by Port 64 Read. Indicates whether the event occurred. 1: Event Occurred 0: Software clears this bit by writing a 1 to the bit location.
		9	R/W1C	0	SMI Caused by Port 60 Write. Indicates whether the event occurred. 1: Event Occurred 0: Software clears this bit by writing a 1 to the bit location.
		8	R/W1C	0	SMI Caused by Port 60 Read. Indicates whether the event occurred. 1: Event Occurred 0: Software clears this bit by writing a 1 to the bit location.

		7	R/W	0	SMI at End of Pass-through Enable. May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later. 1: Enable 0: Disable
		6	RO	0	Pass Through State. 1: Indicates that the state machine is in the middle of an A20GATE pass-through sequence. 0: If software needs to reset this bit, it should set bit 5 to 0.
		5	R/W	0	A20Gate Pass-Through Enable. 1: Allows A20GATE sequence Pass-Through function. SMI# will not be generated, even if the various enable bits are set. 0: Disable
		4	R/W	0	SMI on USB IRQ Enable 1: USB interrupt will cause an SMI event. 0: Disable
		3	R/W	0	SMI on Port 64 Writes Enable. 1: A write to port 64h will cause an SMI event. 0: Disable
		2	R/W	0	SMI on Port 64 Reads Enable. 1: A read to port 64h will cause an SMI event. 0: Disable
		1	R/W	0	SMI on Port 60 Writes Enable. 1: A write to port 60h will cause an SMI event. 0: Disable
		0	R/W	0	SMI on Port 60 Reads Enable. 1: A read to port 60h will cause an SMI event. 0: Disable
Serial ROM Control	0xF0h (UHCI0 only)	4	RO	x	Output of Serial ROM.
		3	R/W	0	ROMDI
		2	R/W	0	ROMCS
		1	R/W	0	ROMSK
		0	R/W	0	Reserved

4.1.2 Funcion 3 Enhanced Host Controller Interface

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Device ID	0x02h	15:0	RO	0x8084h	Genesys Logic EHCI's device ID
Vendor ID	0x00h	15:0	RO	0x17A0h	Genesys Logic's Vendor ID
Command	0x04h	15:10	RO	000000b	Reserved
		9	RO	0b	GL880S doesn' t support Fast Back-to-Back cycle.
		8	R/W	0b	SERRJ Enable: This bit is an enable bit for the SERRJ driver. 0: Disables the SERRJ driver 1: Enables the SERRJ driver
		7	RO	0b	Reserved
		6	R/W	0b	Parity Error Response: This bit controls the device' s response to parity errors. 0: The device sets its Detected Parity Error status bit (bit15 in the Status register) when an error is detected, but doesn't assert PERRJ and continues normal operation 1: The device must take its normal action when a parity error is detected. GL880S will not assert PERRJ when this bit=1.
		5	RO	0b	GL880S does not support palette snoop cycles.
		4	RO	0b	GL880S does not support Memory Write and Invalidate Command
		3	RO	0b	GL880S does not support Special Cycles.
		2	R/W	0b	Bus Master: Controls a device's ability to act as a master on the PCI bus. 0: Disables the device from generating PCI accesses 1: Allows the device to behave as a bus master
		1	R/W	0b	Memory Space: Controls a device's response to Memory space accesses. 0: Disables the device response 1: Allows the device to respond to Memory space accesses
		0	RO	0b	EHCI does not support IO access.
Status	0x06h	15	R/W1C	0b	Detected Parity Error: This bit is set by GL880S whenever it detects a parity error even if parity error handling is disabled.
		14	R/W1C	0b	Signaled System Error: This bit is set whenever GL880S detected SERRJ event, but will not assert SERRJ signal.
		13	R/W1C	0b	Received Master Abort: This bit is set by GL880S whenever its transaction is terminated with Master-Abort.
		12	R/W1C	0b	Received Target Abort: This bit is set by GL880S whenever its transaction is terminated with Target-Abort.

		11	R/W1C	0b	Signaled Target Abort: This bit is set by GL880S whenever it terminates a transaction with Target-Abort.
		10:9	RO	01b	DEVSEL timing: GL880S support medium decode.
		8	R/W1C	0b	Master Data Parity Error: This bit is only implement by bus masters. It is set when three conditions are met: (1) The bus agent asserted PERRJ itself (on a read) or observed PERRJ asserted (on a write); (2) The agent setting the bit acted as the bus master for the operation in which the error occurred; (3) The Parity Error Response bit (Command register) is set.
		7	RO	0b	Fast Back-to-Back Capable: Fast Back-to-Back is not supported.
		6	RO	0b	Reserved
		5	RO	0b	GL880S does not support 66MHz operation.
		4	RO	1b	Capability List: GL880S implement Power Management capability.
		3:0	RO	0000b	Reserved
Class Code	0x09h	23:16	RO	0ch	BaseClass: Serial Bus Controller Device
		15:8	RO	03h	SubClass USB Device
		7:0	RO	20h	Interface Enhanced Host Controller
Revision ID	0x08h	7:0	RO	00h	Version 0.0
BIST	0x0fh	7:0	RO	00h	BIST is not supported
Header Type	0x0eh	7:0	RO	80h	PCI Multi-function device
Latency Timer	0x0dh	7:0	R/W	00h	Latency Timer for this PCI bus master
Cache Line Size	0x0ch	7:0	R/W	00h	Cache Line Size
Base Address Register	0x10h	31:8	R/W	000h	Corresponds to I/O address signals AD[15:5] respectively.
		7:3	RO	00000b	Reserved
		2:0	RO	000b	Base address register field in this register maps to memory space.
Subsystem ID	0x2eh	15:0	RO	0000h	Indicates Subsystem ID
Subsystem Vender ID	0x2ch	15:0	RO	0000h	Indicates Subsystem Vender ID
Capability Pointer	0x34h	7:0	RO	40h	Power Management Capability List header
Max_Lat	0x3fh	7:0	RO	00h	Frequency request of PCI access
Min_Gnt	0x3eh	7:0	RO	00h	Minimum request for burst period
Interrupt Pin	0x3dh	7:0	RO	01h	Routing to INTAJ
Interrupt Line	0x3ch	7:0	R/W	ffh	Indicates interrupt line's route
PMC	0x42h	15	RO	0b	Indicates whether D3cold is supported or not.

		14:11	RO	1111b	PMEJ can be asserted from D0, D1, D2, D3hot.
		10	RO	1b	D2_Support: Support D2 Power Management State
		9	RO	1b	D1_Suport: Support D1 Power Management State
		8:6	RO	00b	Aux_Current Indicates current requirement If PMEJ generation from D3cold is not supported by this host controller core, this field must return a value of "000b" when read. If PMEJ generation from D3cold is supported by this host controller core, following assignments apply: Bit Vaux 8 7 6 Max.CurrentRequired 1 1 1 375mA 1 1 0 320mA 1 0 1 270mA 1 0 0 220mA 0 1 1 169mA 0 1 0 100mA 0 0 1 55mA 0 0 0 0mA
		5	RO	0b	Does not required Specific Initialization before the generic class device driver is able to use it.
		4	RO	0b	Reserved
		3	RO	0b	PME Clock: PCICLK is not required for PMEJ assertion
		2:0	RO	010b	Version: PCI Power Management Interface Specification release 1.1
Next Pointer	0x41h	7:0	RO	00h	No next item in the list
Capability ID	0x40h	7:0	RO	01h	PCI Power Management Interface
PMCSR	0x44h	15	R/W1C	0b	PME_Status: This bit is set to "1" when the function would normally assert PMEJ sugnal independent of the state of the PME_En bit. Writing a "1" to this bit will clear it and cause the function to stop asserting a PMEJ(if enabled). Writing a "0" has no effect.
		14:13	RO	00b	Data_Scale: Data register is not implemented.
		12:9	RO	0000b	Data_Select: Data register is not implemented.
		8	R/W	0b	PME_En: Enable to assert PMEJ. 0b: PMEJ assertion disable 1b: PMEJ assertion enable This bit default to "0" if the host controller core does not support PMEJ generation from D3cold. If the host controller core supports PMEJ generation from D3cold, then this bit is sticky and must be explicitly cleared by the OS each time it is initially loaded.
		7:2	RO	00h	Reserved

		1:0	R/W	00b	Power State: It shows power state of a host controller core and sets the host controller core into a new power state. 00b: D0 01b: D1 10b: D2 11b: D3hot
SBRN	0x60h	7:0	RO	20h	Serial Bus Specification Release Number 2.0
FLADJ	0x61h	7:6	RO	00b	Reserved
		5:0	R/W	20h	Frame Length Timing Value: Default SOF cycle time is 60000h
PORTWAK ECAP	0x62h	15:0	R/W	00h	Port wake capabilities (1:2) ports are to be used for wake events.
EHCI Legacy Support Capabiity	0xC0h	31:25	RO	0h	Reserved
		24	R/W	0	HC OS Owned Semaphore System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as one and the *HC BIOS Owned Semaphore* bit reads as zero.
		23:17	RO	0	Reserved
		16	R/W	0	HC BIOS Owned Semaphore The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to a zero in response to a request for ownership of the EHCI controller by system software.
		15:8	RO	0	Next EHCI Capability Pointer. No other capability is implemented in GL880S.
		7:0	RO	01	Capability ID: current capability is EHCI Legacy Support Capability.
USB Legacy Support/ Control Status	C4h	31	W1C	0	SMI on BAR. This bit is set to one whenever the Base Address Register (BAR) is written.
		30	W1C	0	SMI on PCI Command. This bit is set to one whenever the PCI Command Register is written.
		29	W1C	0	SMI on OS Ownership Change. This bit is set to one whenever the *HC OS Owned Semaphore* bit in the USBLEGSUP register transitions from 1 to a 0 or 0 to a 1
		28:22	RO	0	Reserved
		21	RO	0	SMI on Async Advance. Shadow bit of the *Interrupt on Async Advance* bit in the USBSTS register. To set this bit to a zero, system software must write a one to the *Interrupt on Async Advance* bit in the USBSTS register.
		20	RO	0	SMI on Host System Error. Shadow bit of *Host System Error* bit in the USBSTS register. To set this bit to a zero, system software must write a one to the *Host System Error* bit in the USBSTS register.

		19	RO	0	SMI on Frame List Rollover. Shadow bit of *Frame List Rollover* bit in the USBSTS register To set this bit to a zero, system software must write a one to the *Frame List Rollover* bit in the USBSTS register.
		18	RO	0	SMI on Port Change Detect. Shadow bit of *Port Change Detect* bit in the USBSTS register To set this bit to a zero, system software must write a one to the *Port Change Detect* bit in the USBSTS register.
		17	RO	0	SMI on USB Error Shadow bit of *USB Error Interrupt* (USBERRINT) bit in the USBSTS register To set this bit to a zero, system software must write a one to the *USB Error Interrupt* bit in the USBSTS register.
		16	RO	0	SMI on USB Complete Shadow bit of *USB Interrupt* (USBINT) bit in the USBSTS register To set this bit to a zero, system software must write a one to the *USB Interrupt* bit in the USBSTS register.
		15	R/W	0	SMI on BAR Enable When this bit is one and SMI on BAR Enable When this bit is one and SMI on BAR is one, then GL880S will issue an SMI.
		14	R/W	0	SMI on PCI Command Enable. When this bit is one and SMI on PCI Command is one, then GL880S will issue an SMI.
		13	R/W	0	SMI on OS Ownership Enable When this bit is a one AND the OS Ownership Change bit is one, GL880S will issue an SMI.
		12:6	RO	0	Reserved
		5	R/W	0	SMI on Async Advance Enable. When this bit is a one, and the *SMI on Async Advance* bit (above) in this register is a one, GL880S will issue an SMI immediately.
		4	R/W	0	SMI on Host System Error Enable When this bit is a one, and the *SMI on Host System Error* bit (above) in this register is a one, GL880S will issue an SMI immediately.
		3	R/W	0	SMI on Frame List Rollover Enable. When this bit is a one, and the *SMI on Frame List Rollover* bit (above) in this register is a one, GL880S will issue an SMI immediately.
		2	R/W	0	SMI on Port Change Enable. When this bit is a one, and the *SMI on Port Change Detect* bit (above) in this register is a one, GL880S will issue an SMI immediately.
		1	R/W	0	SMI on USB Error Enable. When this bit is a one, and the *SMI on USB Error* bit (above) in this register is a one, GL880S will issue an SMI immediately.
		0	R/W	0	USB SMI Enable When this bit is a one, and the *SMI on USB Complete* bit (above) in this register is a one, GL880S will issue an SMI immediately.

4.2 UHCI0/UHCI1 Operational Registers Descriptions

4.2.1 USBCMD - USB Command Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x00h	15:8	RO	0x00h	Reserved
Max Packet (MAXP)		7	R/W	0b	This bit selects the maximum packet size that can be used for full speed bandwidth reclamation at the end of a frame. This value is used by GL880S to determine whether it should initiate another transaction based on the time remaining in the SOF counter. 1: 64 bytes. 0:32 bytes.
Configure Flag (CF)		6	R/W	0b	HCD software sets this bit as the last action in its process of configuring GL880S.
Software Debug (SWDBG)		5	R/W	0b	In SW Debug mode, GL880S clears the Run/Stop bit after the completion of each USB transaction. The next transaction is executed when software sets the Run/Stop bit back to 1. 1: Debug mode. 0: Normal Mode.
Force Global Resume (FGR)		4	R/W	0b	1: GL880S sends the Global Resume signal on the USB. 0: Leave resume state.
Enter Global Suspend Mode (EGSM)		3	R/W	0b	1: GL880S enters the Global Suspend mode. 0: Leave global suspend mode
Global Reset (GRESET)		2	R/W	0b	When this bit is set, GL880S sends the global reset signal on USB and then resets all its logic, including the internal hub registers.
Host Controller Reset (HCRESET)		1	R/W	0b	When this bit is set, GL880S resets its internal timers, counters, state machines, etc. to their initial value.
Run/Stop (RS)		0	R/W	0b	1: Run. 0: Stop.

4.2.2 USBSTS - USB Status Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x02h	15:6	RO	0x000h	Reserved
HCHalted		5	R/W1C	0b	GL880S sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by GL880S (debug mode or an internal error).
Host Controller Process Error		4	R/W1C	0b	GL880S sets this bit to 1 when it detects a fatal error and indicates that GL880S suffered a consistency check failure while processing a Transfer Descriptor.
Host System Error		3	R/W1C	0b	GL880S sets this bit to 1 when a serious error occurs during a host system access.

Resume Detect		2	R/W1C	0b	GL880S sets this bit to 1 when it receives a "RESUME" signal from a USB device.
USB Error Interrupt		1	R/W1C	0b	GL880S sets this bit to 1 when completion of a USB transaction results in an error condition.
USB Interrupt (USBINT)		0	R/W1C	0b	GL880S sets this bit to 1 when the cause of an interrupt is a Completion of a USB transaction whose Transfer Descriptor had its IOC bit set.

4.2.3 USBINTR - USB Interrupt Enable Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x04h	15:4	RO	0x000h	Reserved
Short Packet Interrupt Enable		3	R/W	0b	1: Enabled. 0: Disabled.
Interrupt On Complete (IOC) Enable		2	R/W	0b	1: Enabled. 0: Disabled.
Resume Interrupt Enable		1	R/W	0b	1: Enabled. 0: Disabled.
Timeout/CRC Interrupt Enable		0	R/W	0b	1: Enabled. 0: Disabled

4.2.4 FRNUM - Frame Number Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x06h	15:11	RO	0x00h	Reserved
Frame List Current Index/Frame Number		10:0	R/W	0x000h	This register provides the frame number in the SOF Frame. The value in this register increments at the end of each time frame (approximately every 1 ms).

4.2.5 FLBASEADD - Frame List Base Address Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Base Address	0x08h	31:12	R/W	0x00000h	These bits correspond to memory address signals [31:12], respectively.
Reserved		11:0	RO	0x000h	Reserved

4.2.6 Start of Frame (SOF) Modify Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x0ch	7	RO	0b	Reserved
SOF Timing Value		6:0	R/W	0x40h	The SOF cycle time (number of SOF counter clock periods to generate a SOF frame length) is equal to 11936 + value in this field. The default value is decimal 64 which gives a SOF cycle time of 12000.

4.2.7 PORTSC - Port Status and Control Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	(0x10h-0x11h)—Port1 (0x12h-0x13h)—Port2	15:13	RO	000b	Reserved
Suspend		12	R/W	0b	This bit should not be written to a 1 if global suspend is active (bit 3=1 in the USBCMD register). 1: Port in suspense state. 0: Port not in suspense state.
Reserved		11:10	RO	00b	Reserved
Port Reset		9	R/W	0b	1: Port is in Reset. 0: Port is not in Reset.
Low Speed Device Attached		8	RO	0b	1: Low speed device is attached to this port. 0: Full speed device. Writes have no effect.
Reserved		7	RO	1b	Reserved
Resume Detect		6	R/W	0b	1: Resume detected/driven on port. 0: No resume (K-state) detected/ driven on port.
Line Status		5:4	RO	00b	These bits reflect the D+ (bit 4) and D- (bit 5) signals lines' logical levels.
Port Enable/Disable Change		3	R/W1C	0b	1: Port enabled/disabled status has changed. 0: No change.
Port Enable/Disable		2	R/W	0b	1: Enable. 0: Disable.
Connect Status Change		1	R/W1C	0b	Indicates a change has occurred in the port' s Current Connect Status (see bit 0). 1: Change in Current Connect Status. 0: No change.
Current Connect Status		0	RO	0b	This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 1: Device is present on port. 0: No device is present.

4.3 EHCI Operational Registers Descriptions

4.3.1 HCIVERSION / CAPLENGTH Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Interface Version Number	0x00	31:16	RO	0x0100H	Complies with EHCI 1.0
Reserved		15:8	RO	0x0H	Reserved
Capability Registers Length		7:0	RO	0x20H	Offset address for the beginning of operational registers.

4.3.2 HCSPARAMS Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0x04	31:24	RO	0h	Reserved
Debug Port Number		23:20	RO	0h	GL880S does not support debug port.
Reserved		19:17	RO	0h	Reserved
Port Indicators (P_INDICATOR)		16	RO	1b	GL880S support the port indicator control.
Number of Companion Controller (N_CC)		15:12	RO	1h	GL880S implement 1 UHCI.
Number of Portrs per Companion Controller (N_PCC)		11:8	RO	2h	Indicates the number of ports supported companion UHCI.
Port Routing Rules		7	RO	1b	The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP_PORTROUTE array.
Reserved		6:5	RO	0h	Reserved
Port Power Control (PPC)		4	RO	1b	GL880S have port power switches.
Number of Ports (N_PORTS)		3:0	RO	2h	GL880S implements 2 ports.

5.3.3 HCCPARAMS Capability Parameters Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	08H	31:16	RO	0000h	Reserved
EHCI Extended Capability Pointer (EECP)		15:8	RO	C0h	GL880S implements Legayc Support Capability.
Isochronous Scheduling Threshold		7:4	RO	1h	GL880S holds one micro-frame of isochronous data structure.
Reserved		3	RO	0h	Reserved
Asynchronous Schedule Park Capability		2	RO	1	GL880S support asynchronous park function.
Programmable Frame List Flag		1	RO	1b	GL880S supports programmable frame list length.
64-bit Addressing Capability		0	RO	0b	GL880S doesnot support 64-bit addressing mode.

4.3.4 HCSP - PORTROUTE Companion Port Route Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	0CH	31:16	RO	0000h	Reserved
Companion Port Route		15:0		0000h	Port 1, and 2 are routed to UHCI 0.

4.3.5 USBCMD - USB Command Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	20H	31:24	RO	0h	Reserved
Interrupt Threshold Control		23:16	R/W	08h	Indicates the maximum rate at which HC will issue interrupts. Value Maximum Interrupt Interval 00h: Reserved 01h: 1 micro-frame 02h: 2 micro-frames 04h: 4 micro-frames 08h: 8 micro-frames (1 ms) 10h: 16 micro-frames (2 ms) 20h: 32 micro-frames (4 ms) 40h: 64 micro-frames (8 ms) Any other value yields undefined result.
Reserved.		15:12	RO	0h	Reserved
Asynchronous Schedule Park Mode Enable		11	R/W	1b	Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is a zero, Park mode is disabled.

Reserved		10	RO	0h	Reserved
Asynchronous Schedule Park Mode Count		9:8	R/W	3h	This register indicates the count of the number of successive transactions GL880S is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Software must not write a zero to this bit when Park Mode Enable is a one.
Light Host Controller Reset		7	R/W	0h	This bit allows driver to reset EHCI without affecting the state of port or relationship to companion host controller. A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it is safe for host software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host Controller Reset has not yet completed.
Interrupt on Async Advance Doorbell (IOAADB)		6	R/W	0b	This bit is used as a doorbell by software to tell GL880S to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When GL880S has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS register. GL880S sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Asynchronous Schedule Enable		5	R/W	0b	This bit controls whether GL880S skips processing the Asynchronous Schedule.
Periodic Schedule Enable		4	R/W	0b	This bit controls whether the host controller skips processing the Periodic Schedule.
Frame List Size		3:2	R/W	0h	This field specifies the size of the frame list. The size of the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. 00b: 1024 elements (4096 bytes) 01b: 512 elements (2048 bytes) 10b: 256 elements (1024 bytes) – 11b: Reserved
Host Controller Reset (HCRESET)		1	R/W	0b	This bit is used by software to reset GL880S. When software writes a one to this bit, GL880S resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). This bit is set to zero by GL880S when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. HCD should not set this bit to a one when the HCHalted bit is a zero.

Run/Stop (RS)		0	R/W	0b	When set to a 1, GL880S proceeds with execution of the schedule. GL880S continues execution as long as this bit is set to a 1. When this bit is set to 0, GL880S completes the current and any actively pipelined transactions on the USB and then halts.

4.3.6 USBSTS Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	24H	31:16	RO	0h	Reserved
Asynchronous Schedule Status		15	RO	0b	The bit reports the current real status of the Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled.
Periodic Schedule Status		14	RO	0b	The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled.
Reclamation		13	RO	0b	This is a read-only status bit, which is used to detect an empty asynchronous schedule.
HCHalted		12	RO	0b	This bit is a zero whenever the Run/Stop bit is a one. GL880S sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by GL880S.
Reserved.		11:6	RO	0h	Reserved.
Interrupt on Async Advance		5	R/W1C	0b	This bit indicates the GL880S assert interrupt and the source is from IOAADB of USBCMD.
Host System Error		4	R/W1C	0b	GL880S sets this bit to 1 when a serious error occurs during a host system access involving it. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, GL880S clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
Frame List Rollover		3	R/W1C	0b	GL880S sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size.
Port Change Detect		2	R/W1C	0b	GL880S sets it to a one when any port for which the Port Owner bit in the PORTSC[n] register is set to zero is observes the following conditions: 1) A change bit of port transitions from a zero to a one. 2) A PORTSC[n] register Force Port Resume bit of port transitions from a zero to a one as a result of a J-K transition detected on a suspended port.

USB Error Interrupt (USBERRINT)		1	R/W1C	0b	GL880S sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set.
USB Interrupt (USBINT)		0	R/W1C	0b	GL880S sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. GL880S also sets this bit to 1 when a short packet is detected.

4.3.7 USBINTR - USB Interrupt Enable Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	28H	31:6	RO	0h	Reserved
Interrupt on Async Advance Enable		5	R/W	0b	When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, GL880S will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
Host System Error Enable		4	R/W	0b	When this bit is a one, and the Host System Error Status bit in the USBSTS register is a one, GL880S will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
Frame List Rollover Enable.		3	R/W	0b	When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, GL880S will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
Port Change Interrupt Enable.		2	R/W	0b	When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, GL880S will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
USB Error Interrupt Enable.		1	R/W	0b	When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, GL880S will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
USB Interrupt Enable.		0	R/W	0b	When this bit is a one, and the USBINT bit in the USBSTS register is a one, GL880S will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

4.3.8 FRINDEX - Frame Index Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	2CH	31:14	RO	0x0h	Reserved
Frame Index.		13:0	R/W	0000h	The value in this register increments at the end of each time frame (e.g. micro-frame). Bits [N:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register. USBCMD[Frame List Size] Number Elements N 00b (1024) 12 01b (512) 11 10b (256) 10 11b Reserved

4.3.9 CTRLDSSEGMENT - Control Data Structure Segment Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
CTRLDSSEGMENT	30H	31:0	RO	0x0h	GL880S does not support 64-bit addressing mode.

4.3.10 PERIODICLISTABASE Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved.	34H	31:12	RO	0h	Reserved
BaseAddress		11:0	R/W	000h	These bits correspond to memory address signals [31:12], respectively.

4.3.11 ASYNCLISTADDR Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Link Pointer Low	38H	31:5	R/W	0h	These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH),
Reserved.		4:0	RO	0h	Reserved.

4.3.12 CONFIGFLAG - Configure Flag Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved.	60H	31:1	RO	0x0h	Reserved
Configure Flag (CF)		0	R/W	0b	This bit controls the default port-routing control logic. 0b: Port routing control logic default-routes each port to an implementation dependent classic host controller. 1b: Port routing control logic default-routes all ports to this host controller.

4.3.13 PORTSC1~4 - Port Status and Control Registers

Register	Address	Bit	R/W/W1C	Default Value	Descriptions
Reserved	64H, 68H, 6CH, 70H	31:23	RO	0x0h	Reserved
Wake on Over-current Enable (WKOC_E)		22	R/W	0b	Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events.
Wake on Disconnect Enable (WKDSCNNT_E)		21	R/W	0b	Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
Wake on Connect Enable (WKCNNT_E)		20	R/W	0b	Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.
Port Test Control		19:16	R/W	0h	When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE 0010b Test K_STATE 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE
Port Indicator Control.		15:14	R/W	0h	Writing to this bit has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If P_INDICATOR bit is a one, then the bit encodings are: Bit Value Meaning 00b: Port indicators are off 01b: Amber 10b: Green 11b: Undefined
Port Owner		13	R/W	0b	This bit unconditionally goes to a zero when the Configured Flag bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to a one whenever the Configured Flag bit is zero. HCD uses this field to release ownership of the port to a selected HC. HCD writes a one to this bit when the attached device is not a high-speed device.
Port Power (PP)		12	R/W	0b	The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register.

Line Status		11:10	RO	00b	These bits reflect the current logical levels of the D+ (bit 11) and D-(bit 10) signal lines. High-speed device attached: 00b: Receiver squelched 10b: J-state 01b: K-state 11b: Undefined Low/Full-speed device attached 00b: SE0 or open 10b: Full-speed device attached 01b: Low-speed device attached 11b: Undefined This value of this field is undefined if PP bit (Bit 12) is zero.
Reserved.		9	RO	0b	Reserved
Port Reset		8	R/W	0b	1: Port is in Reset. 0: Port is not in Reset.
Suspend		7	R/W	0b	1: Port is in suspense state. 0: Port is not in suspense state.
Force Port Resume		6	R/W		1: Resume detected/driven on port. 0: No resume (K-state) detected/driven on port.
Over-current Change		5	R/W1C	0b	This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
Over-current Active		4	RO	0b	1: This port currently has an over-current condition. 0: This port does not have an over-current condition.
Port Enable/Disable Change		3	R/W1C	0b	1: Port enabled/disabled status has changed. 0: No change.
Port Enabled/ Disabled		2	R/W	0b	Ports can only be enabled by HC as a part of the reset and enable. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by HCD.
Connect Status Change		1	R/W	0b	Indicates a change has occurred in the port's Current Connect Status bit.
Current Connect Status		0	RO	0b	This value reflects the current state of the port. 1: Device is present on port. 0: No device is present.

CHAPTER 5 BLOCK DIAGRAM

5.1 Block Diagram

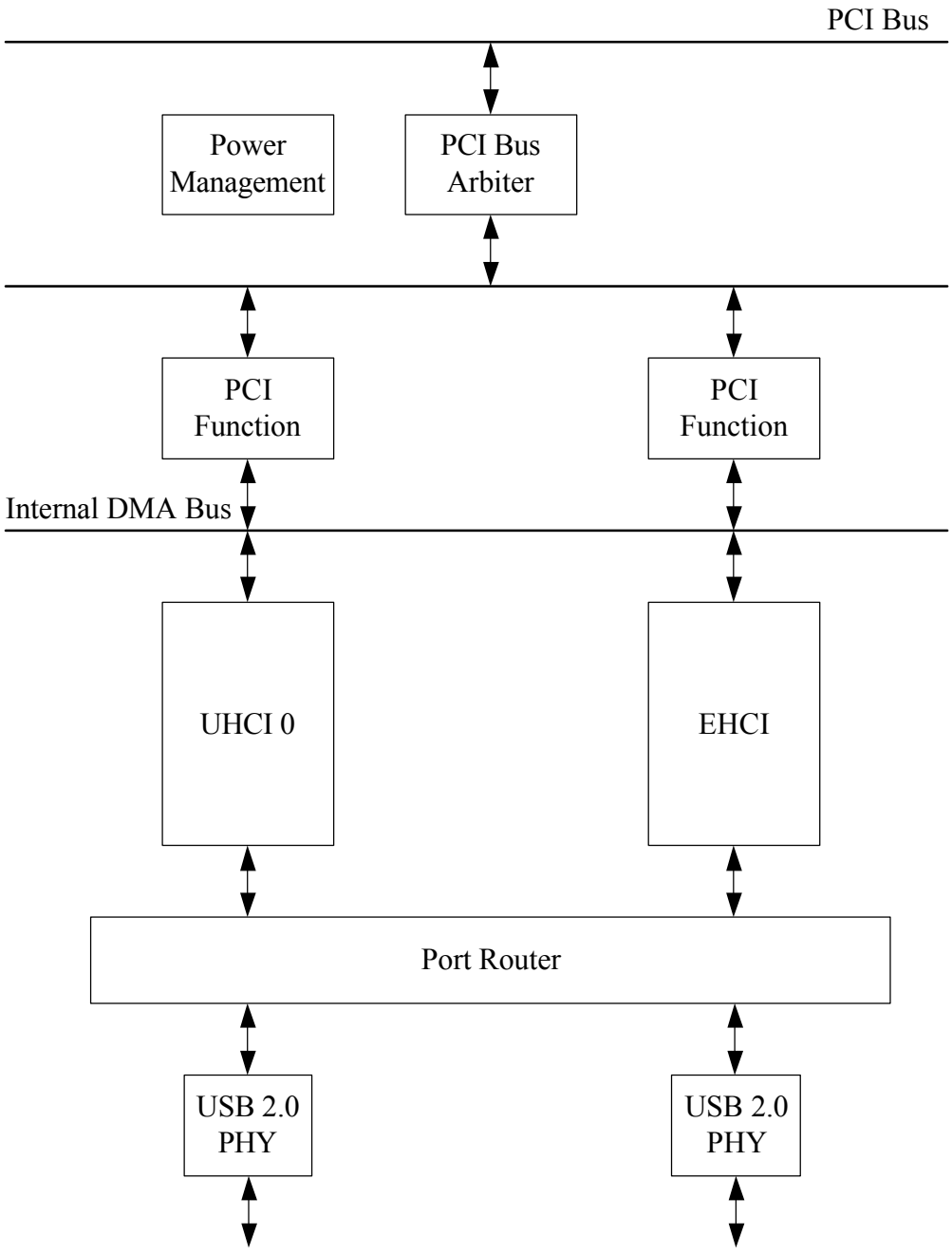

Figure 5.1 - Block Diagram

5.2 Application Diagram

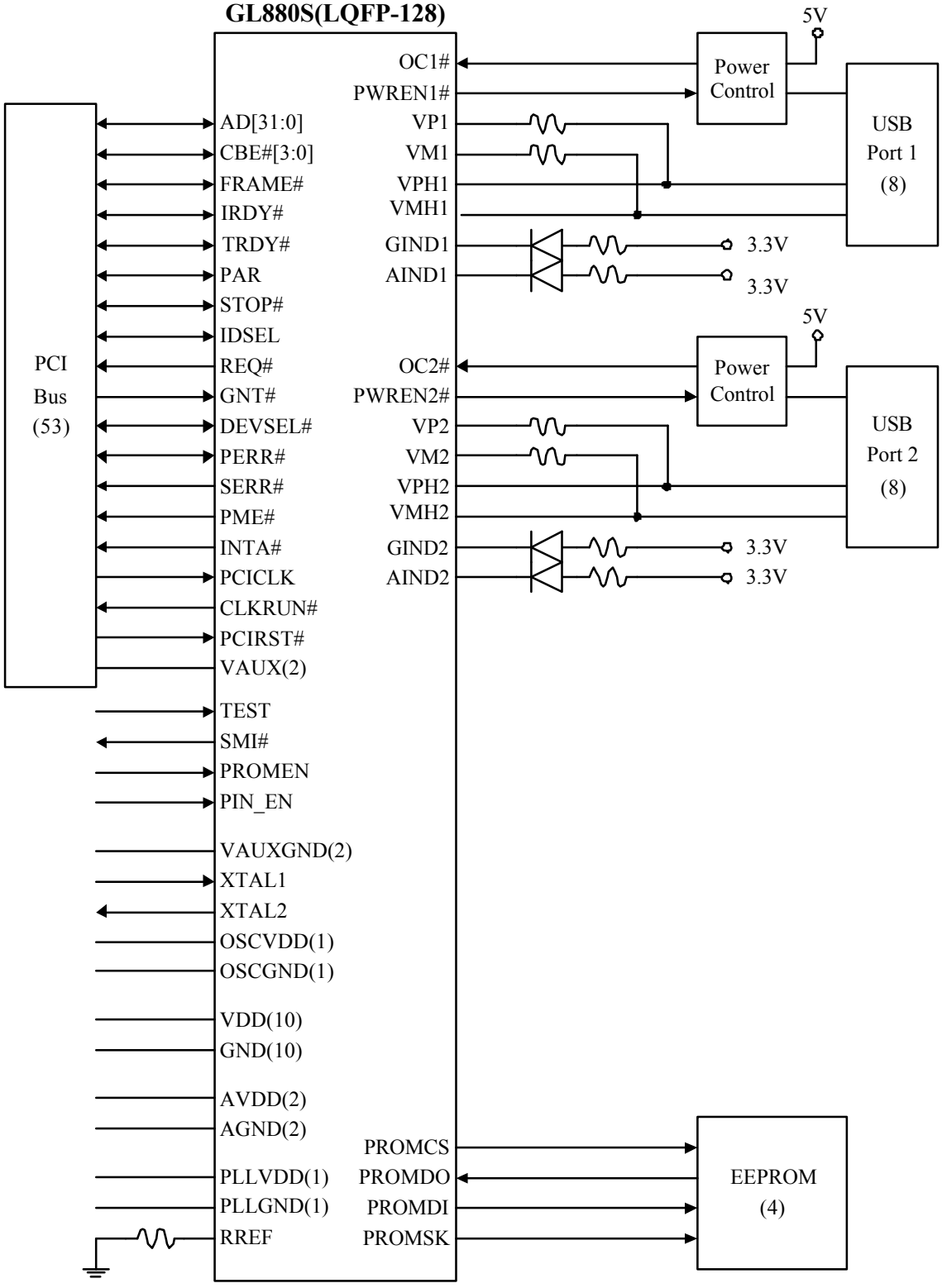

Figure 5.2 - Application Diagram

CHAPTER 6 FUNCTIONAL DESCRIPTION

6.1 Power Management

The GL880S supports the following power management functions:

- Supports different power management states and generation of Power Management Event. GL880S is compliant with PCI Power Management Specification 1.1.
- Supports PCI CLKRUNJ signals, as specified in PCI Mobile Design Guide 1.1, for stop of PCI clock dynamically.

6.1.1 Power Management State and Power Management Event Support

The GL880S supports D0, D1, D2, D3Hot, and D3 Cold power states. D0 is normal power state while D1/D2/D3x support power reduction to different extent. In D3Cold state, Vcc can be removed to save power consumption to the most extent. However, Vaux must be supplied to enable transition back to D0 when wakeup event occurred.

To enable GL880S to enter D3Cold state, the input pin PIN_EN must be keep low before enter, and after leave D3Cold state. In other states (D0/D1/D2/D3Hot), PIN_EN must be kept high under state.

GL880S can assert PMEJ when some given events occur. This is similar to remote wakeup in normal operation. These wakeup events include device connect, device disconnect, remote wakeup, over current, or power state transition. Please note that the Run/Stop bit of UHCI/EHCI must be reset (Stop) before modify the power state to leave D0 state.

6.1.2 PCI CLKRUNJ Support

The GL880S supports PCI CLKRUNJ signal stopping PCI clock dynamically. This function is controlled by CRUNEN (bit 8 of address 0x50H, UHCI0 PCI configuration space.) Default value of CRUNEN is zero, i.e., stop of PCI clock is not allowed. System software or BIOS should set CRUNEN to one before attempt to stop PCI clock.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 7.1 - Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power Supply	-0.5	+3.6	V
V_{IN}	Input Voltage	-0.5	5.5	V
V_{OUT}	Output Voltage	-0.5	+3.6	V
T_A	Ambient Temperature under bias	-60	+100	^{O}C
F_{OSC}	Frequency	12 MHz ±100ppm		Hz

7.2 DC Characteristics

Table 7.2 - DC Characteristics Except USB Signals

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Input Low Voltage	-	0.9	V
V_{IH}	Input High Voltage	2.0	-	V
V_{OL}	Output Low Voltage	-	0.4	V
V_{OH}	Output High Voltage	2.4	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	30	uA

Table 7.3 - DC Characteristics of USB Signals Under FS/LS Mode

Symbol	Parameter	Min.	Max.	Unit
V_{OL}	DPF/DMF static output LOW	-	0.3	V
V_{OH}	DPF/DMF static output HIGH	2.8	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	V
V_{CM}	Differential common mode range	0.8	2.5	V
V_{SE}	Single-end receiver threshold	0.2	-	V
C_{IN}	Transceiver capacitance	-	20	pF
I_{LO}	Hi-Z state data line leakage	-10	+10	uA
Z_{DRV}	Driver output resistance	28	43	Ω

Table 7.4 - DC Characteristics of USB Signals Under HS Mode

Symbol	Parameter	Min.	Max.	Unit
V_{OL}	DPH/DMH static output LOW		0.3	V
V_{OH}	DPH/DMH static output HIGH	2.8	3.6	V
C_{IN}	Transceiver capacitance		20	pF
I_{LO}	Hi-Z state data line leakage	-10	+10	uA

7.3 Power Specifications

Table 7.5 - Power Specifications (1)

	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{TOTAL} (mA)
Low Speed (Mouse)	65.8	69.86	135.66
Full Speed (Flash driver)	65.52	70	135.52
High Speed (HDD)	84.2	88	172.22

***Only one port in operation, the other port is unconnected**

Table 7.6 - Power Specifications (2)

	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{TOTAL} (mA)
Low Speed (Mouse)	69.2	65	134.2
Full Speed (Flash driver)	71	67	138
High Speed (HDD)	105.53	101.4	206.63

*** Two ports in operation, simultaneously**

CHAPTER 8 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.17 (7)	0.22 (9)	0.27 (11)
c	0.09 (4)		0.20 (8)
D	22.00 (866) BSC		
D1	20.00 (787) BSC		
E	16.00 (630) BSC		
E1	14.00 (551) BSC		
e	0.50 (20) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026/BHB
2. ALL DIMENSIONS IN MILLIMETERS.

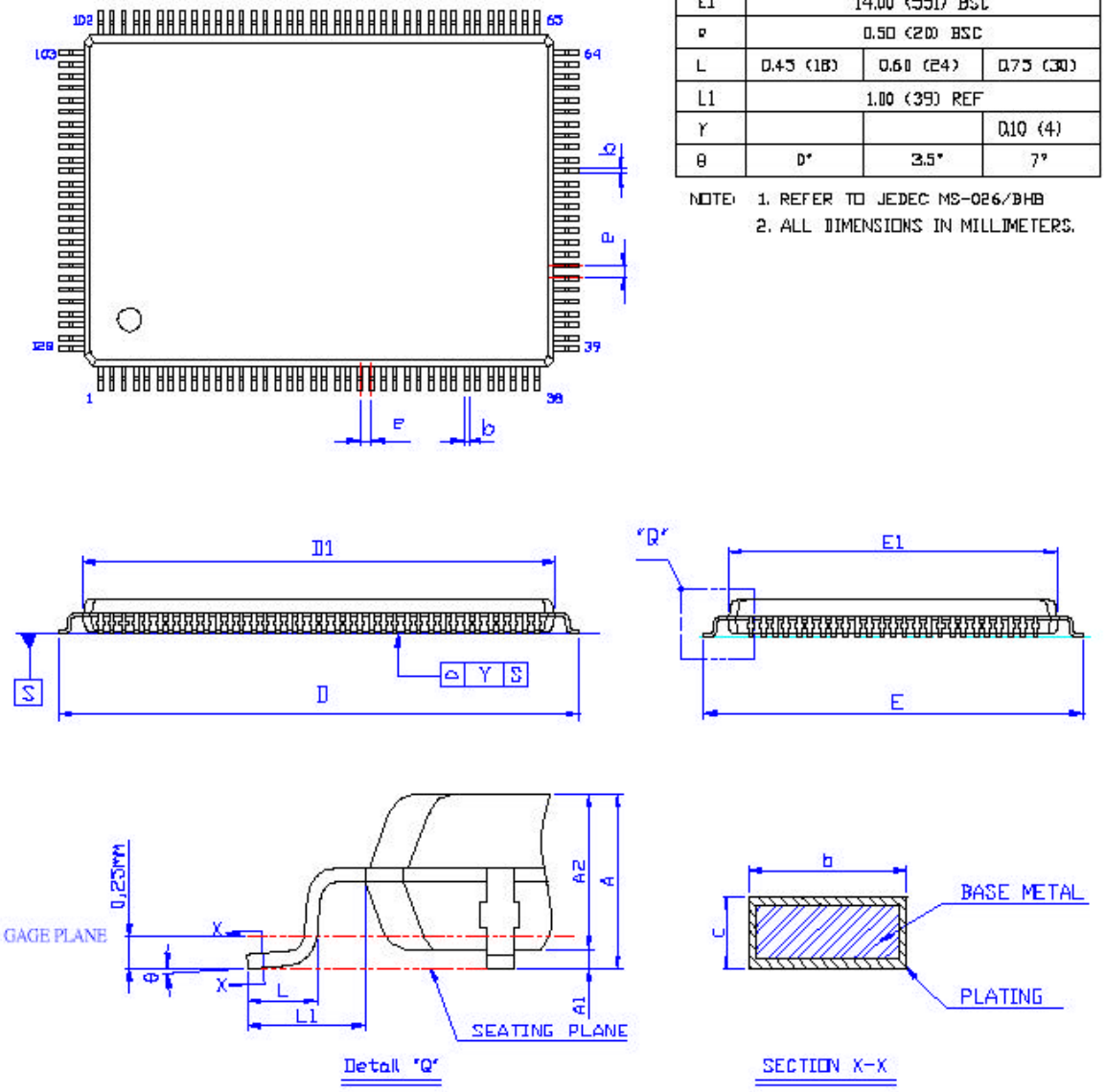

Figure 8.1 - GL880S 128 Pin LQFP Package

CHAPTER 9 ORDERING INFORMATION

Table 9.1 - Ordering Information

Part Number	Package	Status
GL880S	128-pin LQFP	