Si3220/Si3225 Programmer's Guide

Si3220/Si3225 RAM & Register Space

The Si3220/Si3225 is a highly-programmable telephone linecard solution that uses internal registers and RAM to program operational parameters and modes. The register and RAM space are explained in this application note. The register summary and RAM summary are compressed listings for single-entry quick reference. The register descriptions and RAM descriptions give detailed information for each register or RAM location's bits.

All RAM locations are cleared upon hardware reset. All RAM locations that are listed as "INIT" must be initialized to a meaningful value for proper ProSLIC functionality. Bit 4 of the MSTRSTAT register indicates the clearing process is finished. This bit should be checked before initializing the RAM space. Follow the initialization instructions as detailed in "Dual ProSLIC Initialization" .

Accessing register and RAM space is performed through the SPI. Register space is accessed by using the standard three-byte access as described in the Si3220/Si3225 data sheet. Bit 5 of the control byte specifies register access when set to 1. All register space is comprised of 8-bit data.

RAM Access by Register

RAM space can be accessed by two different methods.

One method utilizes three registers in sequence while monitoring RAMSTAT register (bit 0). These three registers are RAMADDR, RAMDATLO, and RAMDATHI.

To read a RAM location in the Si3220/Si3225, check for register RAMSTAT (bit 0) to indicate the previous access is complete and RAM is ready (0). Then, write the RAM address to RAMADDR (RAMSTAT (bit 0) will set to 1). Once RAMSTAT (bit 0) is cleared to 0, the 16 bits of data can be read from the RAMDATLO and RAMDATHI registers.

To write a RAM location in the Si3220/Si3225, check for register RAMSTAT (bit 0) to indicate the previous access is completed and RAM is ready (0). Then, write the 16 bits of RAM data to the RAMDATLO and RAMDATHI registers. Finally, write the RAM address to the RAMADDR register.

RAM Access by Pipeline

An alternative method is a pipeline method that employs a 4-byte access plus a RAM status check. The control byte for the pipeline method has bit 6 cleared to 0 to indicate a RAM access. The control byte is followed by the RAM address byte, then the two data bytes.

Reading RAM in the pipeline method requires "priming" the data. First, check for register RAMSTAT (bit 0) to indicate the previous access is complete and RAM is ready (0). Then, perform the 4-byte RAM access. The first read will yield unusable data. The data read on the subsequent read access is the data for the previous address read. A final address read yields the last previously-requested data. The RAM-ready information (RAMSTAT) must be read before every RAM access.

To write a RAM location, check for register RAMSTAT (bit 0) to indicate the previous access is complete and RAM is ready (0). Then, write the RAM address and data in the 4-byte method. A write to the RAM location requires "priming" the data with subsequent accesses. This method is not more efficient than the access-by-register method.

Chip Select

For register or RAM space access, there are three ways to use chip select: Byte-length, 16-bit length, and access duration length. The byte-length method releases chip select after every eight bits of communication with the Si3220/Si3225. The time between chip select assertions must be at least 220 ns.

The 16-bit length chip select method is similar to the byte-length method except that 16 bits are communicated with the Si3220/Si3225. This means that Si3220/Si3225 communication consists of a control byte, address byte for one 16-bit access, and two data bytes for a second 16-bit access. In a single data byte communication (control byte, address byte, data byte), the data byte should be loaded into either the high byte or both bytes of the second 16-bit access for a write. The 8-bit data exists in the high and low byte of a 16-bit access for a read. The time between chip select assertions must be at least 220 ns.

Access duration length allows chip select to be asserted low for the length of a number of Si3220/Si3225

accesses. There are two very specific rules to this type of communication. First, the SCLK must be of a frequency that is less than 1/2 x 220 ns (<2.25 MHz). Second, access must be done in a 16-bit modulus. This 16-bit modulus follows the same rules as described above for 16-bit length access where 8-bit data is concerned.

Protected Register Bits

The Si3220/Si3225 has protected register bits that are meant to retain the integrity of the Si3220/Si3225 circuit in the event of unintentional software register access. To access the user-protected bits, write the following sequence of data bytes to register address 87 (0x57):

0x02

0x10

0x12

0x00

Following the modification of any protected bit, the same sequence should be immediately written to return these bits to their protected state.

Protected bits exist in registers RLYCON, SBIAS, and THERM. Protected bits can be read at any time.

Dual ProSLIC Initialization

Certain commands must be issued to the Dual ProSLIC to prepare it for operation. The device ID should be read as reference for proper revision-specific operation. Appropriate initial values are then written to all 16-bit RAM locations. Alternate functional values can be written to 8-bit registers if desired. Interrupts are to be cleared and enabled. Finally, the calibration sequence should be followed to prepare the Dual ProSLIC for optimal operation.

1. Ensuring that the RESET pin is held low, apply power.
2. Ensure enough time for the PCLK and FSYNC signals to be present and stable (>300 ms).
3. Preset CS to the high state.
4. CS must be de-asserted for 250 ns min. between accesses.
5. Release the RESET pin to high.
6. Verify PLL achieves lock within 5 ms by ensuring bits 2–4 in MSTRSTAT are set.
7. Read identification register of each device (ID).
8. Write operational values to all 16-bit RAM locations (RAMSTAT).
9. Write alternate values to 8-bit, initialization register locations.

   a.Set power mode (THERM, PTH12, PLPFQ12)

   b.Set two-wire impedance synthesis filter (ZZ, ZRS, ZBxx, ZAxx).

   c.Set channel gain control (AUDGAIN).

   d.Set loop current limit (ILIM).

   e.Set PCM bus mode and clock slot (PCMMODE, PCMTX, PCMRX).

   f.Set tone oscillator parameters (O1Txx, O2Txx, OMODE).

   g.Set tone detectors (TONDEN).

   h.Set ringing configuration (RINGCON, RINGTxx).

   i.Set pulse metering generator (PMTxx).

   j.Set polarity reversal type (POLREV).

   k.Set SLIC bias (SBIAS).
10. Perform all calibrations except common mode, DAC offset, and ADC offset on each channel sequentially (CALR2 = 0x38, CALR1 = 0xBF).
11. Poll CALR1 for calibration complete (CALR1=0x00).
12. Common Mode Balance Calibration. Refer to “Dual ProSLIC Calibration” below.
14. Clear and enable interrupts (IRQ1, IRQ2, IRQ3, IRQEN1, IRQEN2, IRQEN3).
15. Set to Active mode (LINEFEED, LCRRTP).

Dual ProSLIC Calibration

The Dual ProSLIC calibration sequence consists of SLIC mode calibration, monitor ADC calibration, and audio path calibration. The calibration bits that are set in registers CALR1 and CALR2 are executed in order of MSB to LSB for each sequential register. CALR1, bit 7, starts the calibration sequence. CALR2 calibration bits should be set before the CALR1 is written. The reserved bit (bit 6) of CALR1 must always be cleared to 0. The interrupt bit, bit 7 of IRQ3, will report any error in the calibration process. The error could include the line becoming off-hook during the common mode balance calibration.

During all calibrations, the calibration engine controls VTIP and VRING to provide the correct external voltage conditions for the calibration algorithm. The TIP and RING leads must not be connected to ground during any calibration.

The leakage calibrations (CALR1, bits 4–5) can be done at regular intervals to provide optimal performance over temperature variations. The TIP/RING leakage calibrations can be performed every hour. Invoke these leakage calibrations, only during on-hook, by setting CALR1 to 0xB0. The leakage calibration takes 5 ms and interferes with dc feed and voice transmission during its process.

Dual ProSLIC Common Mode Calibration

To optimize common mode (longitudinal) balance performance, it is recommended that the user perform the following steps when running the common mode calibration routine.

1. Write the RAM location values shown in Table 1.
2. Write the Registers values as shown in Table 2. These coefficient values select a 600 Ω impedance synthesis.
3. Ensure phone line is on-hook.
   a.Set LINEFEED = ACTIVE.
   b.Set VOC = 0x2668.
   c.Read LCRRTP and ensure that the line is on-hook. Do not perform this calibration until the line is on-hook.
4. Discharge line
   a.Set VCM and VOC = 0x00.
   b.Wait until VTIP and VRING report 0x00.
5. Set LINEFEED = OPEN.
6. Set Common Mode Balance Interrupt (IRQEN3 = 0x80).
7. Set CALR2 = 0x01. This enables only the AC longitudinal balance calibration routine (CALCMBAL).
8. Set CALR1 = 0x80. This begins the calibration process.
9. Wait for the CALR1 register to clear to 0x00, indicating the longitudinal balance calibration is complete (up to 300ms).
10. Ensure that a common mode balance error interrupt from step 6 did not occur. Retry calibration if true.
11. Rewrite desired RAM and register values that were changed during this calibration.

During all calibrations, the calibration engine controls VTIP and VRING to provide the correct external voltage conditions for the calibration algorithm. The TIP and RING leads must not be connected to ground during any calibration. Note that the channel being calibrated must be on-hook.

Table 1. RAM Values for 600 Ω Impedance, Test Filters and Test Signal

RAM Location Name	Location (decimal)	Value (hexadecimal)
RXGAIN	71	0x4000
TXGAIN	72	0x4000
TXEQCO3	73	0x0050
TXEQCO2	74	0xF8A8
TXEQCO1	75	0x4978
TXEQCO0	76	0x0000
RXEQCO3	77	0x0118
RXEQCO2	78	0xFF30
RXEQCO1	79	0xFB20
RXEQCO0	80	0x5748
RXIIRPOL	81	0x3E08
ECCO1	82	0x06B0
ECCO2	83	0x19D0
ECCO3	84	0x1170
ECCO4	85	0xFF88
ECCO5	86	0xFFD8
ECCO6	87	0xFFA8
ECCO7	88	0xFFB0
ECCO0	89	0x0010
ECIIRB0	90	0xFFB8
ECIIRB1	91	0x0028
ECIIRA1	92	0x61E0
ECIIRA2	93	0xDD88
TXHPF1	163	0x3858

Table 1. RAM Values for 600 Ω Impedance, Test Filters and Test Signal (Continued)

TXHPF2	164	0x7748
TXHPF3	165	0xC7A0
TESTB0H1	126	0x0138
TESTB0L1	125	0x3900
TESTB1H1	128	0x0000
TESTB1L1	127	0x0000
TESTB2H1	130	0xFEC0
TESTB2L1	129	0x4700
TESTA1H1	132	0x5568
TESTA1L1	131	0x0370
TESTA2H1	134	0xC430
TESTA2L1	133	0x2100
TESTB0H2	136	0x5568
TESTB0L2	135	0x0460
TESTB1H2	138	0x0000
TESTB1L2	137	0x0000
TESTB2H2	140	0x0000
TESTB2L2	139	0x0000
TESTA1H2	142	0x0000
TESTA1L2	141	0x0000
TESTA2H2	144	0x0000
TESTA2L2	141	0x0000
TESTB0H3	146	0x4000
TESTB0L3	145	0x0000
TESTB1H3	148	0x0000
TESTB1L3	147	0x0000
TESTB2H3	150	0x0000
TESTB2L3	149	0x0000
TESTA1H3	152	0x0000
TESTA1L3	151	0x0000
TESTA2H3	154	0x0000
TESTA2L3	153	0x0000
OSC1FREQ	94	0x2C30
OSC1AMP	95	0xD9
TESTWLN	157	0x0013

Table 2. Register Values for CM Calibration (600 Ω Impedance Synthesis)

Register Name	Register Location (decimal)	Register Value (hexadecimal)
ZRS	33	0x05
ZZ	34	0x01
ZB0LO	35	0x93
ZB0MID	36	0x95
ZB0HI	37	0x0E
ZB1LO	38	0xD6
ZB1MID	39	0x5F
ZB1HI	40	0xF0
ZB2LO	41	0xD9
ZB2MID	42	0x8A
ZB2HI	43	0xF4
ZB3LO	44	0xFD
ZB3MID	45	0x7F
ZB3HI	46	0x0C
ZA1LO	47	0x44
ZA1MID	48	0x49
ZA1HI	49	0x0F
ZA2LO	50	0xA5
ZA2MID	51	0xB6
ZA2HI	52	0xF8
OMODE	58	0x02

Operation Modes

The active state is the normal operating state of a Dual ProSLIC channel. The Dual ProSLIC automatically switches between active on-hook and active off-hook when the loop closure state has been detected and validated. This mode change occurs with appropriately programmed loop closure threshold (OFFHKTH, ONHKTH), debounce (LCRDBI) and low-pass filter (LCRLPF) values while in the active state. The loop closure low-pass filter normally defaults to 0 since no low-frequency metallic or differential component is expected to distort the loop closure measurement. The Dual ProSLIC can be monitored for indication of loop status in the LCRRTP register. The Dual ProSLIC can also be programmed to cause an interrupt upon any change of the loop status indicator. Ringing frequency, amplitude, and cadence during the RINGING state are fully-programmable to provide country-specific ringing modes. The ringing frequency and amplitude coefficients (RINGFREQ, RINGAMP) are calculated by using either the data sheet equations or the Dual ProSLIC LINC software. The ringing cadence can be controlled by the ringing timers, RINGTAx and RINGTIx. Regular cadence, a designated on time and a designated off time, is fully automatic when the timers are enabled during the ringing state. For example, North American ringing cadence is two seconds on and four seconds off. The timers can also be reloaded at specific intervals to create custom cadences. Refer to the Dual ProSLIC demonstration source code for examples of cadenced ringing. Call processing tones, including pulsed metering tones, are generated and controlled by the Dual ProSLIC. Frequency and amplitude coefficients (OSC1x, OSC2x) are used to program the

tone parameters. These coefficients are calculated using the ProSLIC LINC software. On and off time can be controlled either manually or automatically. Automatic control is performed by enabling the oscillator timers in the OCON register. Each oscillator timer can be set to generate an interrupt upon expiration. Refer to the Dual ProSLIC demonstration source code for an example of tone generation. Ground key detection is accomplished using the ground key detector. This detector monitors longitudinal (common-mode) current (LNGS, LONGxTH) and reports detection in register LCRRTP with an optional interrupt (IRQ2). A debounce time constant (LONGDBI) and low-pass filter (LONGLPF) are also programmable to qualify ground key detection. The low-pass filter is typically programmed for 10 Hz to filter the effects of induced longitudinal power line frequency.

Dual ProSLIC Operation

1. Set operation mode (LINEFEED).
2. Poll loop status (LCRRTP).
3. Respond to interrupts (IRQ0, IRQ1, IRQ2, IRQ3).
4. Respond to DTMF and modem tone detection (TONDTMF, TONDET).
5. Generate FSK signaling (FSKDAT).
6. Generate call processing tones (OCON).
7. Generate pulse metering (PMCON).

Dual ProSLIC Diagnostics

1. Measure real-time line voltage and currents (Vxx, Ixx, Pxx).
2. Perform large-scale line voltage diagnostics
3. (DIAG, DIAGDCTH, DIAGDCCO, DIAGACTH, DIAGACCO, DIAGPK).
4. Perform voice band diagnostics
5. (DIAGxx, TESTxx, ADCHPF1, ADCHPF2, ADCHPF3).
6. Control voice path loop back modes (DIGCON).
7. Control tests relays (RELAYCON: bit 0 and 1).

8-Bit Control Register Summary[1,2]

(Ordered alphabetically by mnemonic except in cases of high, medium, and low bytes which are ordered high to low.)

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
Audio													
21	AUDGAIN	Audio Gain Control		ATXMUTE				ARXMUTE			Init	R/W	0x00
Calibration													
11	CALR1	Calibration Register 1	CAL		CALOFFR	CALOFFT	CALOFFRN	CALOFFTN	CALDIFG	CALCMG	Init	R/W	0x3F
12	CALR2	Calibration Register 2			CALLKGR	CALLKGT	CALMADC	CALDACO	CALADCO	CALCMBAL	Init	R/W	0x3F
Diagnostic Tools													
13	DIAG	Diagnostics Tool Enable	IQ2HR	IQ1HR	TSTRING	TXFILT	SDIAG	SDIAGIN[2:0]			Diag	R/W	
Digital Control and Loopback													
22	DIGCON	Digital Control and Loopback Enable	CODECLB	PCMLB	HYBLB	HYBDIS	THPFDIS	RHPFDIS	DTXMUTE	DRXMUTE	Diag	R/W	0x00
FSK Data Byte													
68	FSKDAT	FSK Data Byte	FSKDAT[7:0]								Oper	R/W	0x00
Chip ID													
0	ID	Chip ID		PARTNUM[2:0][4,6]			REV[3:0][4,6]				Init	R	0x—
Loop Current Limit													
10	ILIM	Loop Current Limit				ILIM[4:0]					Init	R/W	0x05
Interrupts													
14	IRQ0	Interrupt Status 0	CLKIRQ[4,6]	IRQ3B[4,6]	IRQ2B[4,6]	IRQ1B[4,6]		IRQ3A[4,6]	IRQ2A[4,6]	IRQ1A[4,6]	Oper	R	0x00
15	IRQ1	Interrupt Status 1	PULSTAS	PULSTIS	RINGTAS	RINGTIS	OS2TAS	OS2TIS	OS1TAS	OS1TIS	Oper	R/W	0x00
16	IRQ2	Interrupt Status 2	RXMDMS	TXMDMS	RAMIRS	DTMFS	VOCTRKS	LONGS	LOOPS	RTRIPS	Oper	R/W	0x00
17	IRQ3	Interrupt Status 3	CMBALS		PQ6S	PQ5S	PQ4S	PQ3S	PQ2S	PQ1S	Oper	R/W	0x00
18	IRQEN1	Interrupt Enable 1	PULSTAE	PULSTIE	RINGTAE	RINGTIE	OS2TAE	OS2TIE	OS1TAE	OS1TIE	Init	R/W	0x00
19	IRQEN2	Interrupt Enable 2	RXMDME	TXMDME	RAMIRE	DTMFE	VOCTRKE	LONGE	LOOPE	RTRIPE	Init	R/W	0x00
20	IRQEN3	Interrupt Enable 3	CMBALE		PQ6E	PQ5E	PQ4E	PQ3E	PQ2E	PQ1E	Init	R/W	0x00
Linefeed Control													
9	LCRRTP	Loop Closure/Ring Trip/ Ground Key Detection			CMH[4]	SPEED[4]	VOCTST[4]	LONGHI[4]	RTP[4]	LCR[4]	Oper	R	0x40
6	LINEFEED	Linefeed		LFS[2:0][4]				LF[2:0]			Oper	R/W	0x00

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]). All data bits are accessed on a per-channel basis unless noted with a "[6]".
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Single-instance data valid for both channels when writing or reading to either channel.
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
SPI													
3	MSTRSTAT	Master Initialization Status				SRCLR[4,6]	PLOCK[4,6]	FSDET[4,6]			Init	R/W	0x00
Oscillators													
61	O1TAHI	Oscillator 1 Active Timer—High Byte	OSC1TA[15:8]								Init	R/W	0x00
60	O1TALO	Oscillator 1 Active Timer—Low Byte	OSC1TA[7:0]								Init	R/W	0x00
63	O1TIHI	Oscillator 1 Inactive Timer—High Byte	OSC1TI[15:8]								Init	R/W	0x00
62	O1TILO	Oscillator 1 Inactive Timer—Low Byte	OSC1TI[7:0]								Init	R/W	0x00
65	O2TAHI	Oscillator 2 Active Timer—High Byte	OSC2TA[15:8]								Init	R/W	0x00
64	O2TALO	Oscillator 2 Active Timer—Low Byte	OSC2TA[7:0]								Init	R/W	0x00
67	O2TIHI	Oscillator 2 Inactive Timer—High Byte	OSC2TI[15:8]								Init	R/W	0x00
66	O2TILO	Oscillator 2 Inactive Timer—Low Byte	OSC2TI[7:0]								Init	R/W	0x00
59	OCON	Oscillator Control	ENSYNC2[4]	OSC2TAEN	OSC2TIEN	OSC2EN	ENSYNC1[4]	OSC1TAEN	OSC1TIEN	OSC1EN	Oper	R/W	0x00
58	OMODE	Oscillator Mode Select	FSKSSEN	ZEROEN2	ROUT2[1:0]		OSC1FSK	ZEROEN1	ROUT1[1:0]		Init	R/W	0x02
PCM Control													
53	PCMMODE	PCM Mode Select	GCILINE[6]	PCLK2X[6]	PCMTRI[6]	PCMEN	ALAW[1:0][6]		PCMF[1:0][6]		Init	R/W	0x15
57	PCMRXHI	PCM RX Clock Slot—High Byte							PCMRX[9:8]		Init	R/W	0x00
56	PCMRXL0	PCM RX Clock Slot—Low Byte	PCMRX[7:0]								Init	R/W	0x00
55	PCMTXHI	PCM TX Clock Slot—High Byte							PCMTX[9:8]		Init	R/W	0x00
54	PCMTXLO	PCM TX Clock Slot—Low Byte	PCMTX[7:0]								Init	R/W	0x00
Pulse Metering													
28	PMCON	Pulse Metering Control	ENSYNC[4,7]			TAEN1[7]	TIEN1[7]	PULSE1[7]			Oper	R/W	0x00
30	PMTAHI	Pulse Metering Oscillator Active Timer—High Byte	PULSETA[15:8][7]								Init	R/W	0x00
29	PMTALO	Pulse Metering Oscillator Active Timer—Low Byte	PULSETA[7:0][7]								Init	R/W	0x00
32	PMTIHI	Pulse Metering Oscillator Inactive Timer—High Byte	PULSETI[15:8][7]								Init	R/W	0x00

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]). All data bits are accessed on a per-channel basis unless noted with a "[6]".
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Single-instance data valid for both channels when writing or reading to either channel.
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
31	PMTILO	Pulse Metering Oscillator Inactive Timer—Low Byte	PULSETI[7:0][7]								Init	R/W	0x00
Polarity Reversal													
7	POLREV	Polarity Reversal Settings					POLREV[4]	VOCZERO	PREN	RAMP	Init	R/W	
RAM Access													
103	RAMADDR	RAM Address	RAMADDR[7:0][6]								Oper	R/W	0x00
102	RAMDATHI	RAM Data—High Byte	RAMDAT[15:8][6]								Oper	R/W	0x00
101	RAMDATLO	RAM Data—Low Byte	RAMDAT[7:0][6]								Oper	R/W	0x00
4	RAMSTAT	RAM Address Status								RAMSTAT[4]	Init	R	0x00
Soft Reset													
1	RESET	Soft Reset							RESETB	RESETA	Init	R/W	0x00
Ringing													
23	RINGCON	Ringing Configuration	ENSYNC[4]	RDACEN[4]	RINGUNB	TAEN	TIEN	RINGEN[4]	UNBPOLR	TRAP	Init	R/W	0x18
25	RINGTAHI	Ringing Oscillator Active Timer—High Byte	RINGTA[15:8]								Init	R/W	0x00
24	RINGTALO	Ringing Oscillator Active Timer—Low Byte	RINGTA[7:0]								Init	R/W	0x00
27	RINGTIHI	Ringing Oscillator Inactive Timer—High Byte	RINGTI[15:8]								Init	R/W	0x00
26	RINGTILO	Ringing Oscillator Inactive Timer—Low Byte	RINGTI[7:0]								Init	R/W	0x00
Relay Configuration													
5	RLYCON	Relay Driver and Battery Switching Configuration	INVRRO[5]	INVBSEL[5]	BSEL[5]	RRAIL	RDOE	RRD/GPO	TRD2	TRD1	Diag	R/W	0xA3
SLIC Bias Control													
8	SBIAS	SLIC Bias Control	STDBY[5]	SQLCH[5]	CAPB[5]	BIASEN[5]	OBIAS[1:0][5]		ABIAS[1:0][5]		Init	R/W	0xE0
Si3200 Thermometer													
72	THERM	Si3200 Thermometer	STAT[4,6]	SEL[5,6]							Oper	R/W	0x05
Tone Detection													
70	TONDET	Modem Tone Detection	FAILCNT[3:0][6]				PASSCNT[3:0][6]				Oper	R/W	0x00
69	TONDTMF	DTMF Detection			VALID[4]	VALTONE[4]	DTMFDIGIT[3:0][4]				Oper	R	0x00
71	TONDEN	Tone Detection Enable						DTMF	RXMDM	TXMDM	Init	R/W	0x00
Impedance Synthesis Coefficients													

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]). All data bits are accessed on a per-channel basis unless noted with a "[6]".
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Single-instance data valid for both channels when writing or reading to either channel.
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
49	ZA1HI	Impedance Synthesis Coeff A1— High Byte	COEFFA1[20:16][6]								Init	R/W	0x0F
48	ZA1MID	Impedance Synthesis Coeff A1—Middle Byte	COEFFA1[15:8][6]								Init	R/W	0x49
47	ZA1LO	Impedance Synthesis Coeff A1—Low Byte	COEFFA1[7:0]								Init	R/W	0x44
52	ZA2HI	Impedance Synthesis Coeff A2—High Byte	COEFFA2[20:16][6]								Init	R/W	0xF8
51	ZA2MID	Impedance Synthesis Coeff A2—Middle Byte	COEFFA2[15:8][6]								Init	R/W	0xB6
50	ZA2LO	Impedance Synthesis Coeff A2—Low Byte	COEFFA2[7:0][6]								Init	R/W	0xA5
37	ZB0HI	Impedance Synthesis Coeff B0—High Byte	COEFFB0[23:16][6]								Init	R/W	0x0E
36	ZB0MID	Impedance Synthesis Coeff B0—Middle Byte	COEFFB0[15:8][6]								Init	R/W	0x95
35	ZB0LO	Impedance Synthesis Coeff B0—Low Byte	COEFFB0[7:0][6]								Init	R/W	0x93
40	ZB1HI	Impedance Synthesis Coeff B1—High Byte	COEFFB1[23:16][6]								Init	R/W	0xF0
39	ZB1MID	Impedance Synthesis Coeff B1—Middle Byte	COEFFB1[15:8][6]								Init	R/W	0x5F
38	ZB1LO	Impedance Synthesis Coeff B1— Low Byte	COEFFB1[7:0][6]								Init	R/W	0xD6
43	ZB2HI	Impedance Synthesis Coeff B2—High Byte	COEFFB2[23:16][6]								Init	R/W	0xF4
42	ZB2MID	Impedance Synthesis Coeff B2—Middle Byte	COEFFB2[15:8][6]								Init	R/W	0x8A
41	ZB2LO	Impedance Synthesis Coeff B2— Low Byte	COEFFB2[7:0][6]								Init	R/W	0xD9
46	ZB3HI	Impedance Synthesis Coeff B3—High Byte	COEFFB3[23:16][6]								Init	R/W	0x0C
45	ZB3MID	Impedance Synthesis Coeff B3—Middle Byte	COEFFB3[15:8][6]								Init	R/W	0x7F
44	ZB3LO	Impedance Synthesis Coeff B3—Low Byte	COEFFB3[7:0][6]								Init	R/W	0xFD
33	ZRS	Impedance Synthesis Analog Real Coeff					RS[3:0][6]				Init	R/W	0x05
34	ZZ	Impedance Synthesis Analog Complex Coeff	ZSDIS[6]	ZSOHT[6]	ZP[1:0][6]				ZZ[1:0][6]		Init	R/W	0x01

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]). All data bits are accessed on a per-channel basis unless noted with a "[6]".
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Single-instance data valid for both channels when writing or reading to either channel.
7. Si3220 only.

8-Bit Control Descriptions

AUDGAIN: Audio Gain Control (Register Address 21)

(Register type: Initialization)

	D7	D6	D5	D4	D3	D2	D1	D0
Name		ATXMUTE				ARXMUTE		
Type	R/W					R/W		

Reset settings = 0x00

Bit	Name	Function
7	Reserved	Reserved bit.
6	ATXMUTE	**Analog Transmit Path Mute.** 0 = Transmit signal passed. 1 = Transmit signal muted.
5:3	Reserved	Reserved bit.
2	ARXMUTE	**Analog Receive Path Mute.** 0 = Receive signal passed. 1 = Receive signal muted.
1:0	Reserved	Reserved bit.

CALR1: Calibration 1 (Register Address 11)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CAL		CALOFFR	CALOFFT	CALOFFRN	CALOFFTN	CALDIFG	CALCMG
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x3F

Bit	Name	Function
7	CAL	**Calibration Control/Status Bit.** Begins system calibration routine. 0 = Normal operation or calibration complete. 1 = Calibration in progress.
6	Reserved	Reserved bit.
5	CALOFFR	**RING Offset Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
4	CALOFFT	**TIP Offset Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALOFFRN	**IRINGN Offset Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALOFFTN	**ITIPN Offset Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALDIFG	**Differential DAC Gain Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALCMG	**Common Mode DAC Gain Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

CALR2: Calibration 2 (Register Address 12)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CALLKGR	CALLKGT	CALMADC	CALDACO	CALADCO	CALCMBAL
Type			R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x3F

Bit	Name	Function
7:6	Reserved	Reserved bit.
5	CALLKGR	**RING Leakage Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
4	CALLKGT	**TIP Leakage Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALMADC	**Monitor ADC Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALDACO	**DAC Offset Calibration.** Calibrates the audio DAC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALADCO	**ADC Offset Calibration.** Calibrates the audio ADC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALCMBAL	**Common Mode Balance Calibration.** Calibrates the ac longitudinal balance. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

DIAG: Diagnostic Tools (Register Address 13)

(Register type: Diagnostics)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ2HR	IQ1HR	TSTRING	TXFILT	SDIAG	SDIAGIN[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		

Reset settings = 0x00

Bit	Name	Function
7	IQ2HR	**Monitor ADC IQ2 High Resolution Enable.** Sets MADC to high resolution range for IQ2 conversion. 0 = MADC not set to high resolution. 1 = MADC set to high resolution.
6	IQ1HR	**Monitor ADC IQ1 High Resolution Enable.** Sets MADC to high resolution range for IQ1 conversion. 0 = MADC not set to high resolution. 1 = MADC set to high resolution.
5	TSTRING	**Test Ringing Generator Enable.** Enables the capability of generating a low level ringing signal for diagnostic purposes. 0 = Test ringing generator disabled. 1 = Test ringing generator enabled.
4	TXFILT	**Transmit Path Audio Diagnostics Filter Enable.** Enables the transmit path diagnostics filters. 0 = Transmit audio path diagnostics filters disabled. 1 = Transmit audio path diagnostics filters enabled.
3	SDIAG	**SLIC Diagnostics Filter Enable.** Enables the SLIC path diagnostics filters. 0 = SLIC diagnostics filters disabled. 1 = SLIC diagnostics filters enabled. (Voice path processing is disabled.)
2:0	SDIAGIN[2:0]	**SLIC Diagnostics Filter Input.** Selects the input to the SLIC diagnostics filter for dc and low frequency line parameters. 000 = TIP voltage. 001 = RING voltage. 010 = Loop voltage, $V_{TIP} – V_{RING}$. 011 = Longitudinal voltage, $(V_{TIP} + V_{RING})/2$. 100 = Loop (metallic) current. 101 = Longitudinal current. 110 = External ringing voltage (Si3225 only). 111 = External ringing current (Si3225 only).

DIGCON: Digital Control and Loopback Enable (Register Address 22)

(Register type: Diagnostic)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CODECLB	PCMLB	HYBLB	HYBDIS	THPFDIS	RHPFDIS	DTXMUTE	DRXMUTE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	CODECLB	**Codec Loopback Mode Enable.** 0 = Codec loopback mode disabled. 1 = Codec loopback mode enabled.
6	PCMLB	**PCM Loopback Mode Enable.** 0 = PCM loopback mode disabled. 1 = PCM loopback mode enabled.
5	HYBLB	**Hybrid Loopback Mode Enable.** 0 = Hybrid loopback mode disabled. 1 = Hybrid loopback mode enabled.
4	HYBDIS	**Hybrid Balance Filter Disable.** 0 = Hybrid balance enabled. 1 = Hybrid balance disabled.
3	THPFDIS	**Transmit Path High Pass Filter Disable.** 0 = Transmit path HPF enabled. 1 = Transmit path HPF disabled.
2	RHPFDIS	**Receive Path High Pass Filter Disable.** 0 = Receive path HPF enabled. 1 = Receive path HPF disabled.
1	DTXMUTE	**Digital Transmit Path Mute.** 0 = Transmit signal passed. 1 = Transmit signal muted.
0	DRXMUTE	**Digital Receive Path Mute.** 0 = Receive signal passed. 1 = Receive signal muted.

FSKDAT: FSK Data Byte (Register Address 68)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKDAT[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	FSKDAT[7:0]	**FSK Data Byte.** This register contains the raw 8-bit FSK data.

ID: Chip Identification (Register Address 0)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		PARTNUM[2:0]			REV[3:0]			
Type	R				R			

Reset settings = 0xxx

Bit	Name	Function
7	Reserved	Reserved bit.
6:4	PARTNUM[2:0]	**Part Number Identification.** 000 = Si3220 001 = Reserved 010 = Si3225 011–111 = Reserved
3:0	REV[3:0]	**Revision Number Identification.** 0001 = Revision A 0010 = Revision B 0011 = Revision C 0100 = Revision D 0101 = Revision E 0110 = Revision F

ILIM: Loop Current Limit (Register Address 10)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				ILIM[4:0]				
Type	R/W							

Reset settings = 0x05

Bit	Name	Function
7:5	Reserved	Reserved bit.
4:0	ILIM[4:0]	**Loop Current Limit.** The value written to this register sets the constant loop current. The value may be set between 18 mA (0x00) and 45 mA (0x20) in 0.875 mA steps.

IRQ0: Interrupt Status 0 (Register Address 14)

(Register type: Operational/single value instance for both channels/Data includes information for individual channel)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLKIRQ	IRQ3B	IRQ2B	IRQ1B		IRQ3A	IRQ2A	IRQ1A
Type	R	R	R	R		R	R	R

Reset settings = 0x00

Read this interrupt to indicate which interrupt status byte, from which channel, has a pending interrupt.

Bit	Name	Function
7	CLKIRQ	**Clock Failure Interrupt Pending.** 0 = No interrupt pending. 1 = Clock failure interrupt pending. Clock failure status indicated in MSTRSTAT register, bits 7:5.
6	IRQ3B	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 3 (IRQ3) for channel B.
5	IRQ2B	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 2 (IRQ2) for channel B.
4	IRQ1B	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 1 (IRQ1) for channel B.
3	Reserved	Reserved bit.
2	IRQ3A	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 3 (IRQ3) for channel A.
1	IRQ2A	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 2 (IRQ2) for channel A.
0	IRQ1A	**Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending in interrupt status byte 1 (IRQ1) for channel A.

IRQ1: Interrupt Status 1 (Register Address 15)

(Register type: Operational/bits writable in GCI mode only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSTAS	PULSTIS	RINGTAS	RINGTIS	OS2TAS	OS2TIS	OS1TAS	OS1TIS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	PULSTAS	**Pulse Metering Active Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
6	PULSTIS	**Pulse Metering Inactive Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
5	RINGTAS	**Ringing Active Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
4	RINGTIS	**Ringing Inactive Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
3	OS2TAS	**Oscillator 2 Active Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
2	OS2TIS	**Oscillator 2 Inactive Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
1	OS1TAS	**Oscillator 1 Active Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
0	OS1TIS	**Oscillator 1 Inactive Timer Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.

IRQ2: Interrupt Status 2 (Register Address 16)

(Register type: Operational/bits writable in GCI mode only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXMDMS	TXMDMS	RAMIRS	DTMFS	VOCTRKS	LONGS	LOOPS	RTRIPS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	RXMDMS	**Receive Path Modem Tone Detect Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
6	TXMDMS	**Transmit Path Modem Tone Detect Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
5	RAMIRS	**RAM Access Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
4	DTMFS	**DTMF Tone Detect Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
3	VOCTRKS	**VOC Tracking Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
2	LONGS	**Ground Key Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
1	LOOPS	**Loop Closure Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
0	RTRIPS	**Ring Trip Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.

IRQ3: Interrupt Status 3 (Register Address 17)

(Register type: Operational/bits writable in GCI mode only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMBALS		PQ6S	PQ5S	PQ4S	PQ3S	PQ2S	PQ1S
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	CMBALS	**Common Mode Balance Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
6	Reserved	Reserved bit.
5	PQ6S	**Power Alarm Q6 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
4	PQ5S	**Power Alarm Q5 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
3	PQ4S	**Power Alarm Q4 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
2	PQ3S	**Power Alarm Q3 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
1	PQ2S	**Power Alarm Q2 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.
0	PQ1S	**Power Alarm Q1 Interrupt Pending.** 0 = No interrupt pending. 1 = Interrupt pending.

IRQEN1: Interrupt Enable 1 (Register Address 18)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSTAE	PULSTIE	RINGTAE	RINGTIE	OS2TAE	OS2TIE	OS1TAE	OS1TIE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	PULSTAE	**Pulse Metering Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
6	PULSTIE	**Pulse Metering Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
5	RINGTAE	**Ringing Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
4	RINGTIE	**Ringing Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
3	OS2TAE	**Oscillator 2 Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
2	OS2TIE	**Oscillator 2 Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
1	OS1TAE	**Oscillator 1 Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	OS1TIE	**Oscillator 1 Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.

IRQEN2: Interrupt Enable 2 (Register Address 19)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXMDME	TXMDME	RAMIRE	DTMFE	VOCTRKE	LONGE	LOOPE	RTRIPE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	RXMDME	**Receive Path Modem Tone Detect Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
6	TXMDME	**Transmit Path Modem Tone Detect Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
5	RAMIRE	**RAM Access Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
4	DTMFE	**DTMF Tone Detect Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
3	VOCTRKE	**VOC Tracking Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
2	LONGE	**Ground Key Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
1	LOOPE	**Loop Closure Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	RTRIPE	**Ring Trip Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.

IRQEN3: Interrupt Enable 3 (Register Address 20)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMBALE		PQ6E	PQ5E	PQ4E	PQ3E	PQ2E	PQ1E
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	CMBALE	**Common Mode Balance Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
6	Reserved	Reserved bit.
5	PQ6E	**Power Alarm Q6 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
4	PQ5E	**Power Alarm Q5 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
3	PQ4E	**Power Alarm Q4 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
2	PQ3E	**Power Alarm Q3 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
1	PQ2E	**Power Alarm Q2 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	PQ1E	**Power Alarm Q1 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.

LCRRTP: Loop Closure/Ring Trip/Ground Key Detection (Register Address 9)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CMH	SPEED	VOCTST	LONGHI	RTP	LCR
Type			R	R	R	R	R	R

Reset settings = 0x40

Bit	Name	Function
7:6	Reserved	Reserved bit.
5	CMH	**Common Mode High Threshold.** Indicates that common mode threshold has been exceeded. 0 = Common mode threshold no exceeded. 1 = Common mode threshold exceeded.
4	SPEED	**Speedup Mode Enable.** 0 = Speedup disabled. 1 = Automatic speedup.
3	VOCTST	**V_{OC} Tracking Status.** Indicates that battery voltage has dropped and V_{OC} tracking is enabled. 0 = V_{OC} tracking threshold not exceeded, $V_{TR\ on\text{-}hook} = V_{OC}$. 1 = V_{OC} tracking threshold exceeded, $V_{TR\ on\text{-}hook} = V_{OCtrack}$.
2	LONGHI	**Ground Key Detect Flag.** 0 = Ground key event has not been detected. 1 = Ground key event has been detected.
1	RTP	**Ring Trip Detect Flag.** 0 = Ring trip event has not been detected. 1 = Ring trip event has been detected.
0	LCR	**Loop Closure Detect Flag.** 0 = Loop closure event has not been detected. 1 = Loop closure event has been detected.

Note: Detect bits are not sticky bits. Refer to interrupt status for interrupt bit history indication.

LINEFEED: Linefeed Control (Register Address 6)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LFS[2:0]				LF[2:0]		
Type	R					R/W		

Reset settings = 0x00

Bit	Name	Function
7	Reserved	Reserved bit.
6:4	LFS[2:0]	**Linefeed Shadow.** This register reflects the actual realtime linefeed status. Automatic operations may cause actual linefeed state transitions regardless of the Linefeed register settings (e.g., when the Linefeed register is in the ringing state, the Linefeed Shadow register will be reflect the ringing state during ringing bursts and OHT state during silent periods between ringing bursts). 000 = Open 001 = Forward Active 010 = Forward On-hook Transmission (OHT) 011 = TIP Open 100 = Ringing 101 = Reverse Active 110 = Reverse On-hook Transmission 111 = RING Open
3	Reserved	Reserved bit.
2:0	LF[2:0]	**Linefeed.** Writing to this register sets the linefeed state. 000 = Open 001 = Forward Active 010 = Forward On-hook Transmission (OHT) 011 = TIP Open 100 = Ringing 101 = Reverse Active 110 = Reverse On-hook Transmission 111 = RING Open

MSTRSTAT: Master Initialization Status (Register Address 3)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				SRCLR	PLOCK	FSDET		
Type	R/W	R/W	R/W	R	R	R	R	R

Reset settings = 0x00

Bit	Name	Function
7:5	Reserved	Reserved bit.
4	SRCLR	**SRAM Clear Status Detect.** 0 = SRAM clear operation not initiated or in progress. 1 = SRAM clear operation has completed.
3	PLOCK	**PLL Lock Detect.** Indicates the internal PLL is locked relative to FSYNC. 0 = PLL has lost lock relative to FSYNC. 1 = PLL locked relative to FSYNC.
2	FSDET	**FSYNC to PCLK Ratio Detect.** Indicates a valid FSYNC to PCLK ratio has been detected. 0 = Invalid FSYNC to PCLK ratio detected. 1 = Correct FSYNC to PCLK ratio present.
1:0	Reserved	Reserved bit.

O1TAHI: Oscillator 1 Active Timer—High Byte (Register Address 61)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1TA[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC1TA[15:8]	**Oscillator 1 Active Timer—High Byte.** This register contains the upper 8 bits of the 16-bit coefficient for the oscillator 1 active timer.

O1TALO: Oscillator 1 Active Timer—Low Byte (Register Address 60)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1TA[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC1TA[7:0]	**Oscillator 1 Active Timer—Low Byte.** This register contains the lower 8 bits of the 16-bit coefficient for the oscillator 1 active timer. 125 μs/LSB

O1TIHI: Oscillator 1 Inactive Timer—High Byte (Register Address 63)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1TI[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC1TI[15:8]	**Oscillator 1 Inactive Timer—High Byte.** This register contains the upper 8 bits of the 16-bit coefficient for the oscillator 1 inactive timer.

O1TILO: Oscillator 1 Inactive Timer—Low Byte (Register Address 62)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1TI[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC1TI[7:0]	**Oscillator 1 Inactive Timer—Low Byte.** This register contains the lower 8 bits of the 16-bit coefficient for the oscillator 1 inactive timer. 125 μs/LSB

O2TAHI: Oscillator 2 Active Timer—High Byte (Register Address 65)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2TA[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC2TA[15:8]	**Oscillator 2 Active Timer—High Byte.** This register contains the upper 8 bits of the 16-bit coefficient for the oscillator 2 active timer.

O2TALO: Oscillator 2 Active Timer—Low Byte (Register Address 64)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2TA[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC2TA[7:0]	**Oscillator 2 Active Timer—Low Byte.** This register contains the lower 8 bits of the 16-bit coefficient for the oscillator 2 active timer. 125 μs/LSB

O2TIHI: Oscillator 2 Inactive Timer—High Byte (Register Address 67)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2TI[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC2TI[15:8]	**Oscillator 2 Inactive Timer—High Byte.** This register contains the upper 8 bits of the 16-bit coefficient for the oscillator 2 inactive timer.

O2TILO: Oscillator 2 Inactive Timer—Low Byte (Register Address 66)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2TI[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	OSC2TI[7:0]	**Oscillator 2 Inactive Timer—Low Byte.** This register contains the lower 8 bits of the 16-bit coefficient for the oscillator 2 inactive timer. 125 μs/LSB

OCON: Oscillator Control (Register Address 59)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSYNC2	OSC2TAEN	OSC2TIEN	OSC2EN	ENSYNC1	OSC1TAEN	OSC1TIEN	OSC1EN
Type	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	ENSYNC2	Reflects actual oscillator 2 enable status.
6	OSC2TAEN	**Oscillator 2 Active Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
5	OSC2TIEN	**Oscillator 2 Inactive Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
4	OSC2EN	**Oscillator 2 Enable.** 0 = Oscillator 2 disabled. 1 = Oscillator 2 enabled.
3	ENSYNC1	Reflects actual oscillator 1 enable status.
2	OSC1TAEN	**Oscillator 1 Active Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
1	OSC1TIEN	**Oscillator 1 Inactive Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
0	OSC1EN	**Oscillator 1 Enable.** 0 = Oscillator 1 disabled. 1 = Oscillator 1 enabled.

OMODE: Oscillator Mode Select (Register Address 58)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKSSEN	ZEROEN2	ROUT2[1:0]		OSC1FSK	ZEROEN1	ROUT1[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	

Reset settings = 0x00

Bit	Name	Function
7	FSKSSEN	**FSK 8-bit Mode Select.** Sends 8-bit FSK data with start and stop bits when enabled. 1 = No start or stop bits send with FSK data. 0 = FSK data sent with start and stop bits.
6	ZEROEN2	**Zero Voltage Turn Off.** 0 = Oscillator 2 turn off instantly at given phase and voltage. 1 = Oscillator 2 turn off on zero voltage level when disabled manually or by active timer expiration.
5:4	ROUT2[1:0]	00 = Oscillator 2 not directed to either path. 01 = Oscillator 2 directed toward PCM interface (TX path). 10 = Oscillator 2 directed toward 2-wire interface (RX path). 11 = Oscillator 2 directed toward PCM and 2-wire interface (TX and RX path).
3	OSC1FSK	**FSK Mode Enable for Oscillator 1.** 0 = Oscillator 1 is in normal voice band mode. 1 = Oscillator 1 is in FSK mode.
2	ZEROEN1	**Zero Voltage Turn Off.** 0 = Oscillator 1 turn off instantly at given phase and voltage. 1 = Oscillator 1 turn off on zero voltage level when disabled manually or by active timer expiration.
1:0	ROUT1[1:0]	00 = Oscillator 1 not directed to either path. 01 = Oscillator 1 directed toward PCM interface (TX path). 10 = Oscillator 1 directed toward 2-wire interface (RX path). 11 = Oscillator 1 directed toward PCM and 2-wire interface (TX and RX path).

PCMMODE: PCM Mode Select (Register Address 53)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GCILINE*	PCLK2X*	PCMTRI*	PCMEN	ALAW[1:0]*		PCMF[1:0]*	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset settings = 0x05

Bit	Name	Function
7	GCILINE	**GCI Linefeed State Transition Control.** Enables the ability to control linefeed state transitions using the C/I bits in the downstream SC channel byte. See the "Automatic Linefeed State Transitions" table in the Si3220/Si3225 data sheet for automatic linefeed state transitions. 0 = Automatic linefeed state transitions enable. 1 = Downstream C/I bits control all linefeed state transitions.
6	PCLK2X	**2X PCLK Enable.** Enables 2X PCLK mode when GCI interface is selected. 0 = 2X PCLK mode disabled. 1 = 2X PCLK mode enabled.
5	PCMTRI	**PCM Tristate.** 0 = DTX tristates on positive edge of PCLK. 1 = DTX tristates on negative edge of PCLK.
4	PCMEN	**PCM Enable.** 0 = PCM bus disabled. 1 = PCM bus enabled.
3:2	ALAW[1:0]	**A-Law Bit Inversion Format.** Selects bit inversion format when using A-law compression. 00 = No bit inversion. 01 = Invert even bits. 10 = Invert odd bits. 11 = Invert all bits.
1:0	PCMF[1:0]	**PCM Format.** Selects PCM compression format. 00 = 8-bit A-law. 01 = 8-bit μ-law. 10 = 8-bit linear. 11 = 16-bit linear.
***Note:** Bits are single instance for both channels; read from either channel yields same value.		

PCMRXHI: PCM Highway Receive Clock Slot—High Byte (Register Address 57)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							PCMRX[9:8]	
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:2	Reserved	Reserved bit.
1:0	PCMRX[9:8]	**PCM Highway Receive Clock Slot—High Byte.** This register contains the upper 2 bits of the 10-bit clock slot for the receive channel of the PCM highway. This register should be set to a static value during initialization.

PCMRXLO: PCM Highway Receive Clock Slot—Low Byte (Register Address 56)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PCMRX[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PCMRX[7:0]	**PCM Highway Receive Clock Slot—High Byte.** This register contains the lower 8 bits of the 10-bit clock slot for the receive channel of the PCM highway. This register should be set to a static value during initialization.

PCMTXHI: PCM Highway Transmit Clock Slot—High Byte (Register Address 55)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							PCMTX[9:8]	
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:2	Reserved	Reserved bit.
1:0	PCMTX[9:8]	**PCM Highway Transmit Clock Slot—High Byte.** This register contains the upper 2 bits of the 10-bit clock slot for the transmit channel of the PCM highway.

PCMTXLO: PCM Highway Transmit Clock Slot—High Byte (Register Address 54)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PCMTX[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PCMTX[7:0]	**PCM Highway Transmit Clock Slot—Low Byte.** This register contains the lower 8 bits of the 10-bit clock slot for the transmit channel of the PCM highway.

PMCON: Pulse Metering Control (Register Address 28)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSYNC			TAEN1	TIEN1	PULSE1		
Type	R			R/W	R/W	R/W		

Reset settings = 0x00

Bit	Name	Function
7	ENSYNC	**Pulse Metering Waveform Present Flag.** Indicates a pulse metering waveform is present. 0 = No pulse metering waveform present. 1 = Pulse metering waveform present.
6:5	Reserved	Reserved bit.
4	TAEN1	**Pulse Metering Active Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
3	TIEN1	**Pulse Metering Inactive Timer Enable.** 0 = Timer disabled. 1 = Timer enabled.
2	PULSE1	**Pulse Metering Enable.** 0 = Pulse metering disabled. 1 = Pulse metering enabled.
1:0	Reserved	Reserved bit.

PMTAHI: Pulse Metering Oscillator Active Timer—High Byte (Register Address 30)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSETA[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PULSETA[15:8]	**Pulse Metering Oscillator Active Timer.** This register contains the upper 8 bits of the pulse metering oscillator active timer. Register 29 contains the lower 8 bits of this value.

PMTALO: Pulse Metering Oscillator Active Timer—Low Byte (Register Address 29)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSETA[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PULSETA[7:0]	**Pulse Metering Oscillator Active Timer.** This register contains the lower 8 bits of the pulse metering oscillator active timer. Register 30 contains the upper 8 bits of this value. 125μs/LSB

PMTIHI: Pulse Metering Oscillator Inactive Timer—High Byte (Register Address 32)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSETI[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PULSETI[15:8]	**Pulse Metering Oscillator Inactive Timer.** This register contains the upper 8 bits of the pulse metering oscillator inactive timer. Register 29 contains the lower 8 bits of this value.

PMTILO: Pulse Metering Oscillator Inactive Timer—Low Byte (Register Address 31)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PULSETI[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	PULSETI[7:0]	**Pulse Metering Oscillator Inactive Timer.** This register contains the lower 8 bits of the pulse metering oscillator inactive timer. Register 30 contains the upper 8 bits of this value. 125μs/LSB

POLREV: Polarity Reversal Settings (Register Address 7)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					POLREV	VOCZERO	PREN	RAMP
Type					R	R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7:4	Reserved	Reserved bit.
3	POLREV	**Polarity Reversal Status.** 0 = Forward polarity. 1 = Reverse polarity.
2	VOCZERO	**Wink Function Control.** Enables a wink function by decrementing the open circuit voltage to zero. 0 = Maintain current V_{OC} value. 1 = Decrement V_{OC} voltage to 0 V.
1	PREN	**Smooth Polarity Reversal Enable.** 0 = Disabled. 1 = Enabled.
0	RAMP	**Smooth Polarity Reversal Ramp Rate.** 0 = 1 V/1.25 ms ramp rate. 1 = 2 V/1.25 ms ramp rate.

RAMADDR: RAM Address (Register Address 103)

(Register type: Operational/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAMADDR[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RAMADDR[7:0]	**RAM Data—Low Byte.** A write to RAMDAT followed by a write to RAMADDR places the contents of RAMDAT into a RAM location specified by the RAMADDR at the next memory update (WRITE operation). Writing RAMADDR loads the data stored in RAMADDR into RAMDAT only at the next memory update (READ operation).

RAMDATHI: RAM Data—High Byte (Register Address 102)

(Register type: Operational/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAMDAT[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RAMDAT[15:8]	**RAM Data—High Byte.** A write to RAMDAT followed by a write to RAMADDR places the contents of RAMDAT into a RAM location specified by the RAMADDR at the next memory update (WRITE operation). Writing RAMADDR loads the data stored in RAMADDR into RAMDAT only at the next memory update (READ operation).

RAMDATLO: RAM Data—Low Byte (Register Address 101)

(Register type: Operational/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAMDAT[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RAMDAT[7:0]	**RAM Data—Low Byte.** A write to RAMDAT followed by a write to RAMADDR places the contents of RAMDAT into a RAM location specified by the RAMADDR at the next memory update (WRITE operation). Writing RAMADDR loads the data stored in RAMADDR only into RAMDAT at the next memory update (READ operation).

RAMSTAT: RAM Address Status (Register Address 4)

(Register type: Operational/Single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								RAMSTAT
Type								R

Reset settings = 0x00

Bit	Name	Function
7:1	Reserved	Reserved bit.
0	RAMSTAT	**RAM Address Status.** 0 = RAM ready for access. 1 = RAM access pending internally (busy).

RESET: Soft Reset (Register Address 1)

(Register type: Initialization/Single value instance for both channels, includes data for individual channel)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RESETB	RESETA
Type							R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7:2	Reserved	Reserved bit.
1	RESETB	**Soft Reset, Channel B.** 0 = Normal operation. 1 = Initiate soft reset to channel B.
0	RESETA	**Soft Reset, Channel A.** 0 = Normal operation. 1 = Initiate soft reset to channel A.
Note: Soft reset set to a single channel of a given device causes all register space to reset to default values for that channel. Soft reset set to both channels of a given device causes a hardware reset including PLL reinitialization and RAM clear.		

RINGCON: Ringing Configuration (Register Address 23)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSYNC	RDACEN	RINGUNB	TAEN	TIEN	RINGEN	UNBPOLR	TRAP
Type	R	R	R/W	R/W	R/W	R	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7	ENSYNC	**Ringing Waveform Present Flag.** 0 = No ringing waveform present. 1 = Ringing waveform present.
6	RDACEN	**Ringing Waveform Sent to Differential DAC.** 0 = Ringing waveform not sent to differential DAC. 1 = Ringing waveform set to differential DAC.
5	RINGUNB	**Unbalanced Ringing Enable.** Enables internal unbalanced ringing generation. 0 = Unbalanced ringing not enabled. 1 = Unbalanced ringing enabled.
4	TAEN	**Ringing Active Timer Enable.** 0 = Ringing active timer disabled. 1 = Ringing active timer enabled.
3	TIEN	**Ringing Inactive Timer Enable.** 0 = Ringing inactive timer disabled. 1 = Ringing inactive timer enabled.
2	RINGEN	**Ringing Oscillator Enable Monitor.** This bit will toggle when the ringing oscillator is enabled and disabled. 0 = Ringing oscillator is disabled. 1 = Ringing oscillator is enabled.
1	UNBPOLR	**Reverse Polarity Unbalanced Ringing Select. The RING of RAM location must be modified from its normal ringing polarity setting. Refer to data sheet for use.** 0 = Normal polarity ringing. 1 = Reverse polarity ringing.
0	TRAP	**Ringing Waveform Selection.** 0 = Sinusoid waveform. 1 = Trapezoid waveform.

RINGTAHI: Ringing Oscillator Active Timer—High Byte (Register Address 25)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGTA[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RINGTA[15:8]	**Ringing Oscillator Active Timer.** This register contains the upper 8 bits of the ringing oscillator active timer (the on-time of the ringing burst). Register 24 contains the upper 8 bits of this value.

RINGTALO: Ringing Oscillator Active Timer—Low Byte (Register Address 24)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGTA[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RINGTA[7:0]	**Ringing Oscillator Active Timer.** This register contains the lower 8 bits of the ringing oscillator active timer (the on-time of the ringing burst). Register 25 contains the upper 8 bits of this value. 125 μs/LSB.

RINGTIHI: Ringing Oscillator Inactive Timer—High Byte (Register Address 27)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGTI[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RINGTI[15:8]	**Ringing Oscillator Inactive Timer.** This register contains the upper 8 bits of the ringing oscillator inactive timer (the silent period between ringing bursts). Register 26 contains the upper 8 bits of this value.

RINGTILO: Ringing Oscillator Inactive Timer—Low Byte (Register Address 26)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGTI[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	RINGTI[7:0]	**Ringing Oscillator Inactive Timer.** This register contains the lower 8 bits of the ringing oscillator inactive timer (the silent time between ringing bursts). Register 27 contains the upper 8 bits of this value. 125 μs/LSB.

RLYCON: Relay Driver and Battery Switching Configuration (Register Address 5)

(Register type: Diagnostic)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INVRRD	INVBSEL	BSEL	RRAIL	RDOE	RRD/GPO	TRD2	TRD1
Type	R/W–P	R/W–P	R/W–P	R/W	R/W	R/W	R/W	R/W

Reset settings = 0xA3

Bit	Name	Function
7	INVRRD	Inverts the polarity of the RRD pin relative to the RRD bit setting. 0 = Active high. 1 = Active low.
6	INVBSEL	Inverts the polarity of the BSEL pin relative to the BSEL bit setting. 0 = Active high. 1 = Active low.
5	BSEL	**Battery Select Indicator.** 0 = BATSEL pin is output low. (Si3200 internal battery switch open) 1 = BATSEL pin is output high.(Si3200 internal battery switch closed)
4	RRAIL	**Additional Ringing Rail Present (Si3200, Third Battery).** 0 = Ringing rail not present. 1 = Ringing rail present. For Si3220, RRD/GPO toggles with LINEFEED ringing cadence.
3	RDOE	**Relay Driver Output Enable.** 0 = Disabled. 1 = Enabled.
2	RRD/GPO	**Ringing Relay Driver Output/General Purpose Output.** 0 = RRD/GPO output low. (Default output at pin is high due to INVRRD = 1 default) 1 = RRD/GPO output high.
1	TRD2	**Test Relay Driver 2 Output.** 0 = TRD2 output low. 1 = TRD2 output high.
0	TRD1	**Test Relay Driver 1 Output.** 0 = TRD1 output low. 1 = TRD1 output high.
Note: Bit type “P” = user-protected bits. Refer to the protected register bit section in the text of this application note.		

SBIAS: SLIC Bias Control (Register Address 8)

(Register type: Initialization/protected register bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STDBY	SQLCH	CAPB	BIASEN	OBIAS[1:0]		ABIAS[1:0]	
Type	R/W–P	R/W–P	R/W–P	R/W–P	R/W–P		R/W–P	

Reset settings = 0xE0

Bit	Name	Function
7	STDBY	**Low-power Standby Status.** Writing to this bit causes temporary manual control of this bit until a subsequent on-hook or off-hook transition. 0 = low-power mode off (ie. Active off-hook). 1 = = low-power mode on (ie. Active on-hook).
6	SQLCH	**Audio Squelch Control.** Indicates squelch of audio during the setting time set by the SPEEDUP RAM coefficient. Writing to this bit causes temporary manual override until a speedup event occurs. 0 = Squelch off. 1 = Squelch on.
5	CAPB	**Audio Filter Capacitor Bypass.** Indicates filter capacitor pass during the setting time set by the SPEEDUP RAM coefficient. Writing to this bit causes temporary manual override until a speedup event occurs. 0 = Capacitors not bypassed. 1 = Capacitors bypassed.
4	BIASEN	**SLIC Bias Enable.** Writing to this bit causes temporary manual control of SLIC bias until a subsequent on-hook or off-hook state. 0 = SLIC bias off (ie. Active on-hook). 1 = = SLIC bias on (ie. Active off-hook).
3:2	OBIAS[1:0]	**SLIC Bias Level, On-Hook Transmission State.** DC bias current flowing in the SLIC circuit during on-hook transmission state. Increasing this value increases the ability of the SLIC to withstand longitudinal current artifacts. 00 = 4 mA per lead. 01 = 8 mA per lead. 10 = 12 mA per lead. 11 = 16 mA per lead.
1:0	ABIAS[1:0]	**SLIC Bias Level, Active State.** DC bias current flowing in the SLIC circuit during the active off-hook state. Increasing this value increases the ability of the SLIC to withstand longitudinal current artifacts. 00 = 4 mA per lead. 01 = 8 mA per lead. 10 = 12 mA per lead. 11 = 16 mA per lead.
Note: Bit type “P” = user-protected bits. Refer to the protected register bit section in the text of this application note.		

THERM: Si3200 Thermometer (Register Address 72)

(Register type: Diagnostic/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STAT	SEL						
Type	R	P						

Reset settings = 0x00

Bit	Name	Function
7	STAT	**Si3200 Thermometer Status.** Reads whether the Si3200 has shut down due to an over-temperature event. 0 = Si3200 operating within normal operating temperature range. 1 = Si3200 has exceeded maximum operating temperature.
6	SEL	**Sensing Mode Selection.** Power sensing mode selection when using the Si3200. (Protected Register Bit) 0 = Transistor power sum used for power sensing (PSUM vs. threshold in PTH12). 1 = Si3200 therm diode used for power sensing.
5:0	Reserved	Reserved bit.
Note: Bit type “P” = User-protected bit. Refer to the register bit section in the text of this application note.		

TONDET: Modem Tone Detection (Register Address 70)

(Register type: Operational/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FAILCNT[3:0]				PASSCNT[3:0]			
Type	R/W				R/W			

Reset settings = 0x00

Bit	Name	Function
7:4	FAILCNT[3:0]	Tone detection failure count threshold –66.25 ms/LSB.
3:0	PASSCNT[3:0]	Tone detection pass count threshold –66.25 ms/LSB

TONDTMF: DTMF Detection (Register Address 69)

(Register type: Operational)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VALID	VALTONE	DTMFDIGIT[3:0]			
Type			R	R	R			

Reset settings = 0x00

Bit	Name	Function
7:6	Reserved	Reserved bit.
5	VALID	0 = valid DTMF digit not pending. 1 = valid DTMF digit pending.
4	VALTONE	0 = No validated DTMF digit. 1 = Validated DTMF digit.
3:0	DTMFDIGIT[3:0]	Binary value of latest validated DTMF digit.

TONDEN: Tone Detection Enable (Register Address 71)

(Register type: Initialization)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DTMF	RXMDM	TXMDM
Type						R/W	R/W	R/W

Reset settings = 0x00

Bit	Name	Function
7:3	Reserved	Reserved bit.
2	DTMF	**DTMF Detection Disable.** 0 = DTMF detection enabled. 1 = DTMF detection disabled.
1	RXMDM	**Receive Path Modem Detection Disable.** 0 = Receive path modem tone detection enabled. 1 = Receive path modem tone detection disabled.
0	TXMDM	**Transmit Path Modem Detection Disable.** 0 = Transmit path modem tone detection enabled. 1 = Transmit path modem tone detection disabled.

ZA1HI: Impedance Synthesis Coefficient A1—High Byte (Register Address 49)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				COEFFA1[20:16]				
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:5	Reserved	**Reserved bit.**
4:0	COEFFA1[20:16]	**Impedance Synthesis Coefficient A1—High Byte.** This register contains the upper 8 bits of the 21-bit A1 impedance synthesis coefficient. Refer to coefficient generation program.

ZA1MID: Impedance Synthesis Coefficient A1—Middle Byte (Register Address 48)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFA1[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFA1[15:8]	**Impedance Synthesis Coefficient A1—Middle Byte.** This register contains the middle 8 bits of the 21-bit A1 impedance synthesis coefficient. Refer to coefficient generation program.

ZA1LO: Impedance Synthesis Coefficient A1—Low Byte (Register Address 47)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFA1[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFA1[7:0]	**Impedance Synthesis Coefficient A1—Low Byte.** This register contains the lower 8 bits of the 21-bit A1 impedance synthesis coefficient. Refer to coefficient generation program.

ZA2HI: Impedance Synthesis Coefficient A2—High Byte (Register Address 52)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				COEFFA2[20:16]				
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:5	Reserved	**Reserved bit.**
4:0	COEFFA2[20:16]	**Impedance Synthesis Coefficient A2—High Byte.** This register contains the upper 5 bits of the 21-bit A2 impedance synthesis coefficient. Refer to coefficient generation program.

ZA2MID: Impedance Synthesis Coefficient A2—Middle Byte (Register Address 51)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFA2[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFA2[15:8]	**Impedance Synthesis Coefficient A2—Middle Byte.** This register contains the middle 8 bits of the 21-bit A2 impedance synthesis coefficient. Refer to coefficient generation program.

ZA2LO: Impedance Synthesis Coefficient A2—Low Byte (Register Address 50)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFA2[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFA2[7:0]	**Impedance Synthesis Coefficient A2—Low Byte.** This register contains the lower 8 bits of the 21-bit A2 impedance synthesis coefficient. Refer to coefficient generation program.

ZB0HI: Impedance Synthesis Coefficient B0—High Byte (Register Address 37)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB0[23:16]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB0[23:16]	**Impedance Synthesis Coefficient B0—High Byte.** This register contains the upper 8 bits of the 24-bit B0 impedance synthesis coefficient. Refer to coefficient generation program.

ZB0MID: Impedance Synthesis Coefficient B0—Middle Byte (Register Address 36)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB0[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB0[15:8]	**Impedance Synthesis Coefficient B0—Middle Byte.** This register contains the middle 8 bits of the 24-bit B0 impedance synthesis coefficient. Refer to coefficient generation program.

ZB0LO: Impedance Synthesis Coefficient B0—Low Byte (Register Address 35)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB0[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB0[7:0]	**Impedance Synthesis Coefficient B0—Low Byte.** This register contains the lower 8 bits of the 24-bit B0 impedance synthesis coefficient. Refer to coefficient generation program.

ZB1HI: Impedance Synthesis Coefficient B1—High Byte (Register Address 40)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB1[23:16]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB1[23:16]	**Impedance Synthesis Coefficient B1—High Byte.** This register contains the upper 8 bits of the 24-bit B1 impedance synthesis coefficient. Refer to coefficient generation program.

ZB1MID: Impedance Synthesis Coefficient B1—Middle Byte (Register Address 39)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB1[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB1[15:8]	**Impedance Synthesis Coefficient B1—Middle Byte.** This register contains the middle 8 bits of the 24-bit B1 impedance synthesis coefficient. Refer to coefficient generation program.

ZB1LO: Impedance Synthesis Coefficient B1—Low Byte (Register Address 38)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB1[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB1[7:0]	**Impedance Synthesis Coefficient B1—Low Byte.** This register contains the lower 8 bits of the 24-bit B1 impedance synthesis coefficient. Refer to coefficient generation program.

ZB2HI: Impedance Synthesis Coefficient B2—High Byte (Register Address 43)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB2[23:16]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB2[23:16]	**Impedance Synthesis Coefficient B2—High Byte.** This register contains the upper 8 bits of the 24-bit B2 impedance synthesis coefficient. Refer to coefficient generation program.

ZB2MID: Impedance Synthesis Coefficient B2—Middle Byte (Register Address 42)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB2[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB2[15:8]	**Impedance Synthesis Coefficient B2—Middle Byte.** This register contains the middle 8 bits of the 24-bit B2 impedance synthesis coefficient. Refer to coefficient generation program.

ZB2LO: Impedance Synthesis Coefficient B2—Low Byte (Register Address 41)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB2[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB2[7:0]	**Impedance Synthesis Coefficient B2—Low Byte.** This register contains the lower 8 bits of the 24-bit B2 impedance synthesis coefficient. Refer to coefficient generation program.

ZB3HI: Impedance Synthesis Coefficient B3—High Byte (Register Address 46)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB3[23:16]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB3[23:16]	**Impedance Synthesis Coefficient B3—High Byte.** This register contains the upper 8 bits of the 24-bit B3 impedance synthesis coefficient. Refer to coefficient generation program.

ZB3MID: Impedance Synthesis Coefficient B3—Middle Byte (Register Address 45)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB3[15:8]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB3[15:8]	**Impedance Synthesis Coefficient B3—Middle Byte.** This register contains the middle 8 bits of the 24-bit B3 impedance synthesis coefficient. Refer to coefficient generation program.

ZB3LO: Impedance Synthesis Coefficient B3—Low Byte (Register Address 44)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	COEFFB3[7:0]							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	COEFFB3[7:0]	**Impedance Synthesis Coefficient B3—Low Byte.** This register contains the lower eight bits of the 24-bit B3 impedance synthesis coefficient. Refer to coefficient generation program.

ZRS: Impedance Synthesis—Analog Real Coefficient (Register Address 33)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					RS[3:0]			
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:4	Reserved	Reserved bit.
3:0	RS[3:0]	**Impedance Synthesis Analog Real Coefficient.** Refer to coefficient generation program.

ZZ: Impedance Synthesis—Analog Complex Coefficient (Register Address 34)

(Register type: Initialization/single value instance for both channels)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ZSDIS	ZSOHT	ZP[1:0]				ZZ[1:0]	
Type	R/W	R/W	R/W				R/W	

Reset settings = 0x00

Bit	Name	Function
7	ZSDIS	**Analog Impedance Synthesis Coefficient Disable.** Enables/disables RS, ZSOHT, ZP, and ZZ coefficients. 0 = Analog Z_{SYNTH} coefficients enabled. 1 = Analog Z_{SYNTH} coefficients disabled.
6	ZSOHT	**Impedance Synthesis Analog Complex Coefficient.** Refer to coefficient generation program.
5:4	ZP[1:0]	
3:2	Reserved	
1:0	ZZ[1:0]	

Internal 16-Bit RAM Summary[1]

(ordered alphabetically by mnemonic)

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
Battery Selection and VOC Tracking																						
31	BATHTH	High Battery Switch Threshold		BATHTH[14:7][2]															Init	0E54	18	V
34	BATLPF	Battery Tracking Filter Coeff	BATLPF[15:3]																Init	0A08	10	Hz
32	BATLTH	Low Battery Switch Threshold		BATLTH[14:7][2]															Init	0D88	17	V
33	BSWLPF	RING Voltage Filter Coeff	BSWLPF[15:3]																Init	0A08	10	Hz
Speedup																						
36	CMHITH	Speedup High Threshold	CMHITH[15:0]																Init	00CB	1	V
35	CMLOTH	Speedup Low Threshold	CMLOTH[15:0]																Init	07F5	10	V
SLIC Diagnostics Filter																						
53	DIAGAC	SLIC Diags AC Detector Threshold	DIAGAC[15:0]																Diag			V
54	DIAGACCO	SLIC Diags AC Filter Coeff	DIAGACCO[15:3]																Diag	7FF8	127.3	Hz
51	DIAGDC	SLIC Diags DC Output	DIAGDC[15:0]																Diag			V
52	DIAGDCCO	SLIC Diags DC Filter Coeff	DIAGDCCO[15:3]																Diag	0A08	10	Hz
55	DIAGPK	SLIC Diags Peak Detector	DIAGPK[15:0]																Diag			V
DTMF Detection																						
118	DTCOL2HTH	DTMF Column Second Harmonic Threshold	DTCOL2HTH[15:3]																Init	1013	—	
116	DTCOLRTH	DTMF Column Ratio Threshold	DTCOLRTH[15:3]																Init	0CC5	—	
112	DTCOLTH	DTMF Column Peak Threshold	DTCOLTH[15:3]																Init	1999	—	
113	DTFTWTH	DTMF Forward Twist Threshold	DTFTWTH[15:3]																Init	1013	—	
120	DTHOTTH	DTMF Hot Limit Threshold	DTHOTTH[15:0]																Init	0A1C	—	
119	DTMINPTH	DTMF Minimum Power Threshold	DTMINPTH[15:0]																Init	00E5	—	
108	DTROW0TH	DTMF Row 0 Peak Threshold	DTROW0TH[15:3]																Init	2AE1	—	
109	DTROW1TH	DTMF Row 1 Peak Threshold	DTROW1TH[15:3]																Init	28F3	—	
117	DTROW2HTH	DTMF Row Second Harmonic Threshold	DTROW2HTH[15:3]																Init	308C	—	
110	DTROW2TH	DTMF Row 2 Peak Threshold	DTROW2TH[15:3]																Init	25C2	—	
111	DTROW3TH	DTMF Row 3 Peak Threshold	DTROW3TH[15:3]																Init	249B	—	
115	DTROWRTH	DTMF Row Ratio Threshold	DTROWRTH[15:3]																Init	0CC5	—	
114	DTRTWTH	DTMF Reverse Twist Threshold	DTRTWTH[15:3]																Init	1013	—	
Echo Cancellation																						

Notes:

1. RAM values are 2's complement unless otherwise noted. Any register not listed is reserved and must not be written.
2. Only positive input values are valid for these RAM addresses.
3. Si3225 only.
4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
89	ECCO0	Echo Cancellation Coeff 0	ECCO0[15:3]																Init	0010	—	
82	ECCO1	Echo Cancellation Coeff 1	ECCO1[15:3]																Init	06B0	—	
83	ECCO2	Echo Cancellation Coeff 2	ECCO2[15:3]																Init	19D0	—	
84	ECCO3	Echo Cancellation Coeff 3	ECCO3[15:3]																Init	1178	—	
85	ECCO4	Echo Cancellation Coeff 4	ECCO4[15:3]																Init	FF88	—	
86	ECCO5	Echo Cancellation Coeff 5	ECCO5[15:3]																Init	FFD8	—	
87	ECCO6	Echo Cancellation Coeff 6	ECCO6[15:3]																Init	FFA8	—	
88	ECCO7	Echo Cancellation Coeff 7	ECCO7[15:3]																Init	FFB0	—	
92	ECIIRA1	Echo Cancel IIR Filter Coeff A1	ECIIRA1[15:3]																Init	61E0	—	
93	ECIIRA2	Echo Cancel IIR Filt Coeff A2	ECIIRA2[15:3]																Init	DD88	—	
90	ECIIRB0	Echo Cancel IIR Filt Coeff B0	ECIIRB0[15:3]																Init	FFB8	—	
91	ECIIRB1	Echo Cancel IIR Filt Coeff B1	ECIIRB1[15:3]																Init	0028	—	
FSK Generation																						
102	FSKAMP0	FSK Amplitude for Space	FSKAMP0[15:3]																Init	222	.22	Vrms
103	FSKAMP1	FSK Amplitude for Mark	FSKAMP1[15:3]																Init	123	.22	Vrms
100	FSKFREQ0	FSK Frequency for Space	FSKFREQ0[15:3]																Init	35B0	1200	Hz
101	FSKFREQ1	FSK Frequency for Mark	FSKFREQ1[15:3]																Init	3CE0	2200	Hz
104	FSK01HI	FSK 0-1 Transition Freq—High	FSK01HI[15:3]																Init	1118		
105	FSK01LO	FSK 0-1 Transition Frequency—Low	FSK01LO[15:3]																Init	1D88		
106	FSK10HI	FSK 1-0 Transition Frequency—High	FSK10HI[15:3]																Init	3BE0		
107	FSK10LO	FSK 1-0 Transition Frequency—Low	FSK10LO[15:3]																Init	1330		
Loop Currents																						
9	ILONG	Longitudinal Current Sense Value	ILONG[15:0][2]																DIag			mA
8	ILOOP	Loop Current Sense Value	ILOOP[15:0][2]																Diag			mA
18	IRING	Q5 Current Measurement	IRING[15:0]																Diag			mA
16	IRINGN	Q3 Current Measurement	IRINGN[15:0]																Diag			mA
15	IRINGP	Q2 Current Measurement	IRINGP[15:0]																Diag			mA
21	IRNGNG	External Ringing Generator Current Measurement	IRNGNG[15:0][3]																Diag			mA
19	ITIP	Q6 Current Measurement	ITIP[15:0]																Diag			mA
17	ITIPN	Q4 Current Measurement	ITIPN[15:0]																Diag			mA
14	ITIPP	Q1 Current Measurement	ITIPP[15:0]																Diag			mA
Loop Closure Detection																						
24	LCRDBI	Loop Closure Detection Debounce Interval	LCRDBI[15:0][2]																Init	000C	15	ms
25	LCRLPF	Loop Closure Filter Coefficient	LCRLPF[15:3]																Init	0A10	10	Hz
26	LCRMASK	Loop Closure Mask Interval Coeff	LCRMASK[15:0][2]																Init	0040	80	ms

Notes:

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2. Only positive input values are valid for these RAM addresses.
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5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
166	LCRMSKPR	LCR Mask During Polarity Reversal	LCRMSKPR[15:0]																Init	0040	80	ms
22	LCROFFHK	Off-Hook Detect Threshold	LCROFFHK[15:0][2]																Init	0F92	12	mA
23	LCRONHK	On-Hook Detect Threshold	LCRONHK[15:0][2]																Init	0C9C	10	mA
Longitudinal Current Detection																						
29	LONGDBI	Ground Key Detection Debounce Interval	LONGDBI[15:0][2]																Init	0020	40	ms
27	LONGHITH	Ground Key Detection Threshold	LONGHITH[15:0][2]																Init	0A17	8	mA
28	LONGLOTH	Ground Key Removal Detection Threshold	LONGLOTH[15:0][2]																Init	08D4	7	mA
30	LONGLPF	Ground Key Filter Coefficient	LONGLPF[15:3]																Init	0A08	10	Hz
Oscillator Coefficients																						
95	OSC1AMP	Oscillator 1 Amplitude	OSC1AMP[15:0]																Init	00D9	0.0687	Vrms
94	OSC1FREQ	Oscillator 1 Frequency	OSC1FREQ[15:3]																Init	2C30	1030	Hz
96	OSC1PHAS	Oscillator 1 Initial Phase	OSC1PHAS[15:0]																Init	0000		
98	OSC2AMP	Oscillator 2 Amplitude	OSC2AMP[15:0]																Init	0063	0.0775	Vrms
97	OSC2FREQ	Oscillator 2 Frequency	OSC2FREQ[15:3]																Init	3C38	440	Hz
99	OSC2PHAS	Oscillator 2 Initial Phase	OSC2PHAS[15:0]																Init	0000		
Power Calculations																						
40	PLPF12	Q1/Q2 Thermal Low-Pass Filter Coeff	PLFP12[15:3]																Init	0066[9]	.4	s
41	PLFP34	Q3/Q4 Thermal Low-Pass Filter Coeff	PLPF34[15:3]																Init	0088	.3	s
42	PLPF56	Q5/Q6 Thermal Low-Pass Filter Coeff	PLPF56[15:3]																Init	000E	3	s
Pulse Metering																						
68	PMAMPL	Pulse Metering Amplitude	PMAMPL[15:0][4]																Init	0880	0.2	V
70	PMAMPTH	Pulse Metering AGC Amplitude Threshold	PMAMPTH[15:0][4]																Init	1562	0.5	V
67	PMFREQ	Pulse Metering Frequency	PMFREQ[15:3][4]																Init	C3EC	12	kHz
69	PMRAMP	Pulse Metering Ramp Rate	PMRAMP[15:0][4]																Init	008A	17	ms
Power Calculations																						
44	PQ1DH	Q1 Calculated Power	PQ1DH[15:0]																Diag			W
45	PQ2DH	Q2 Calculated Power	PQ2DH[15:0]																Diag			W
46	PQ3DH	Q3 Calculated Power	PQ3DH[15:0]																Diag			W
47	PQ4DH	Q4 Calculated Power	PQ4DH[15:0]																Diag			W
48	PQ5DH	Q5 Calculated Power	PQ5DH[15:0]																Diag			W
49	PQ6DH	Q6 Calculated Power	PQ6DH[15:0]																Diag			W
50	PSUM	Total Calculated Power	PSUM[15:0]																Diag			W
37	PTH12	Q1/Q2 Power Threshold	PTH12[15:0][2]																Init	054C[9]	1.44	W
38	PTH34	Q3/Q4 Power Threshold	PTH34[15:0][2]																Init	003C	.17	W
39	PTH56	Q5/Q6 Power Threshold	PTH56[15:0][2]																Init	002A	1.28	W

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5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
43	RB56	Q5/Q6 Base Resistor	RB56[15:0]																Init			Ω
Ringing																						
59	RINGAMP	Ringing Amplitude/Zero Crossing Delay	RINGAMP[15:0][6]/ZERDELAY[15:0]																Init	00CB	45	Vrms
57	RINGFRHI	Ringing Frequency—High Byte/Linefeed Status Delay		RINGFRHI[14:3][5]/LFSDELAY[14:3]															Init	3F78	20	Hz
58	RINGFRLO	Ringing Frequency—Low Byte		RINGFRLO[14:3][4]															Init	6CE8	20	Hz
56	RINGOF	Ringing Waveform DC Offset		RINGOF[14:0][4]															Init	0000	0	V
60	RINGPHAS	Ringing Oscillator Initial Phase	RINGPHAS[15:3][8]																Init	0000		
Ring Trip Detection																						
66	RTACDB	AC Ring Trip Debounce Interval	RTACDB[15:0]																Init	0003	75	ms
64	RTACTH	AC Ring Trip Detect Threshold	RTACTH[15:0]																Init	0FD2	45	mA
61	RTCOUNT	Ring Trip Timeout Counter	RTCOUNT[15:0]																Init	0400	128	ms
65	RTDCDB	DC Ring Trip Debounce Interval	RTDCDB[15:0]																Init	0003	75	ms
62	RTDCTH	DC Ring Trip Detect Threshold	RTDCTH[15:0]																Init	7FFF	∞	mA
63	RTPER	Ring Trip Low-Pass Filter Coeff Period	RTPER[15:0]																Init	0028	40	Hz
Receive Path Gain and Filters																						
81	RXIIRPOL	RX IIR Filter Pole Coeff	RXIIRPOL[15:3]																Init	3E08	—	
80	RXEQCO0	RX Equalizer Coeff 0	RXEQCO0[15:3]																Init	5748	—	
79	RXEQCO1	RX Equalizer Coeff 1	RXEQCO1[15:3]																Init	FB20	—	
78	RXEQCO2	RX Equalizer Coeff 2	RXEQCO2[15:3]																Init	FF30	—	
77	RXEQCO3	RX Equalizer Coeff 3	RXEQCO3[15:3]																Init	0018	—	
71	RXGAIN	RX Gain Setting	RXGAIN[15:3]																Init	4000	0	dB
123	RXMODPWR	RX Path Modem Tone Power	RXMODPWR[15:3]																Init			
121	RXPWR	RX Path Input Signal Power	RXPWR[15:0]																Init			
DC Speedup																						
168	SPEEDUP	DC Speedup Timer	SPEEDUP[15:0][2]																Init	0000	60	ms
169	SPEEDUPR	Ring Speedup Timer	SPEEDUPR[15:0][2]																Init	0000	60	ms
Test Diagnostic Filters																						
132	TESTA1H1	TX Diag Filter Coeff A1H1	TESTA1H1[15:3]																Diag	5568	—	
142	TESTA1H2	TX Diag Filter Coeff A1H2	TESTA1H2[15:3]																Diag	0000	—	
152	TESTA1H3	TX Diag Filter Coeff A1H3	TESTA1H3[15:3]																Diag	0000	—	
131	TESTA1L1	TX Diag Filter Coeff A1L1	TESTA1L1[15:3]																Diag	0376	—	
141	TESTA1L2	TX Diag Filter Coeff A1L2	TESTA1L2[15:3]																Diag	0000	—	
151	TESTA1L3	TX Diag Filter Coeff A1L3	TESTA1L3[15:3]																Diag	0000	—	

Notes:

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2. Only positive input values are valid for these RAM addresses.
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4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
134	TESTA2H1	TX Diag Filter Coeff A2H1	TESTA2H1[15:3]																Diag	C430	—	
144	TESTA2H2	TX Diag Filter Coeff A2H2	TESTA2H2[15:3]																Diag	0000	—	
154	TESTA2H3	TX Diag Filter Coeff A2H3	TESTA2H3[15:3]																Diag	0000	—	
133	TESTA2L1	TX Diag Filter Coeff A2L1	TESTA2L1[15:3]																Diag	2100	—	
143	TESTA2L2	TX Diag Filter Coeff A2L2	TESTA2L2[15:3]																Diag	0000	—	
153	TESTA2L3	TX Diag Filter Coeff A2L3	TESTA2L3[15:3]																Diag	0000	—	
156	TESTAVO	TX Diag Filter Avg Output	TESTAVO[15:0]																Diag			V
158	TESTAVBW	TX Diag Filter Avg Bandwidth	TESTAVBW[15:3]																Diag			
160	TESTAVFL	TX Diag Filter Average Flag	TESTAVFL[15:3]																Diag			
162	TESTAVTH	TX Diag Filter Avg Threshold	TESTAVTH[15:3]																Diag			
126	TESTB0H1	TX Diag Filter Coeff B0H1	TESTB0H1[15:3]																Diag	0138	—	
136	TESTB0H2	TX Diag Filter Coeff B0H2	TESTB1H2[15:3]																Diag	5568	—	
146	TESTB0H3	TX Diag Filter Coeff B0H3	TESTB0H3[15:3]																Diag	4000	—	
125	TESTB0L1	TX Diag Filter Coeff B0L1	TESTB0L1[15:3]																Diag	3900	—	
135	TESTB0L2	TX Diag Filter Coeff B0L2	TESTB0L2[15:3]																Diag	0460	—	
145	TESTB0L3	TX Diag Filter Coeff B0L3	TESTB0L3[15:3]																Diag	0000	—	
128	TESTB1H1	TX Diag Filter Coeff B1H1	TESTB1H1[15:3]																Diag	0000	—	
138	TESTB1H2	TX Diag Filter Coeff B1H2	TESTB1H2[15:3]																Diag	0000	—	
148	TESTB1H3	TX Diag Filter Coeff B1H3	TESTB1H3[15:3]																Diag	0000	—	
127	TESTB1L1	TX Diag Filter Coeff B1L1	TESTB1L1[15:3]																Diag	0000	—	
137	TESTB1L2	TX Diag Filter Coeff B1L2	TESTB1L2[15:3]																Diag	0000	—	
147	TESTB1L3	TX Diag Filter Coeff B1L3	TESTB1L3[15:3]																Diag	0000	—	
130	TESTB2H1	TX Diag Filter Coeff B2H1	TESTB2H1[15:3]																Diag	FEC0	—	
140	TESTB2H2	TX Diag Filter Coeff B2H2	TESTB2H2[15:3]																Diag	0000	—	
150	TESTB2H3	TX Diag Filter Coeff B2H3	TESTB2H3[15:3]																Diag	0000	—	
129	TESTB2L1	TX Diag Filter Coeff B2L1	TESTB2L1[15:3]																Diag	4700	—	
139	TESTB2L2	TX Diag Filter Coeff B2L2	TESTB2L2[15:3]																Diag	0000	—	
149	TESTB2L3	TX Diag Filter Coeff B2L3	TESTB2L3[15:3]																Diag	0000	—	
159	TESTPKFL	TX Diag Filter Peak Flag	TESTPKFL[15:3]																Diag			
155	TESTPKO	TX Diag Filter Peak Output	TESTPKO[15:3]																Diag			V
161	TESTPKTH	TX Diag Filter Peak Threshold	TESTPKTH[15:3]																Diag			
157	TESTWLN	TX Diag Filter	TESTWLN[15:3]																Diag	0013	—	
Transmit Path Gain and Filters																						
76	TXEQCO0	TX Equalizer Coefficient 0	TXEQCO0[15:3]																Init	0000	—	
75	TXEQCO1	TX Equalizer Coefficient 1	TXEQCO1[15:3]																Init	4978	—	
74	TXEQCO2	TX Equalizer Coefficient 2	TXEQCO2[15:3]																Init	F8A8	—	

Notes:

1. RAM values are 2's complement unless otherwise noted. Any register not listed is reserved and must not be written.
2. Only positive input values are valid for these RAM addresses.
3. Si3225 only.
4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Ex. Hex	Ex. Dec	Unit
73	TXEQCO3	TX Equalizer Coefficient 3	TXEQCO3[15:3]																Init	0050	—	
72	TXGAIN	TX Gain Setting	TXGAIN[15:3]																Init	4000	0	dB
163	TXHPF1	TX HPF Coefficient 1	TXHPF1[15:3]																Diag	3858	—	
164	TXHPF2	TX HPF Coefficient 2	TXHPF2[15:3]																Diag	7748	—	
165	TXHPF3	TX HPF Coefficient 3	TXHPF3[15:3]																Diag	C7A0	—	
124	TXMODPWR	TX Path Modem Tone Power	TXMODPWR[15:3]																Init			
122	TXPWR	TX Path Input Signal Power	TXPWR[15:0]																Init			
Loop Voltages																						
13	VBAT	Scaled Battery Voltage Measurement	VBAT[15:0]																Diag			V
4	VCM	Common Mode Voltage		VCM[14:0][2]															Init	0268	3	V
7	VLOOP	Loop Voltage	VLOOP[15:0][2]																Diag			V
0	VOC	Open Circuit Voltage		VOC[14:0][2]															Init	2668	48	V
1	VOCDELTA	VOC Delta for Off-Hook		VOCDELTA[14:0][2]															Init	0592	7	V
3	VOCHTH	VOC Delta Upper Threshold	VOCHTH[15:0][2]																Init	0197	2	V
2	VOCLTH	VOC Delta Lower Threshold	VOCLTH[15:0][2]																Init	F9A2	–8	V
10	VOCTRACK	Battery Tracking Open Circuit Voltage	VOCTRACK[15:0][2]																Diag			V
5	VOV	Overhead Voltage		VOV[14:0][2]															Init	032F	4	V
6	VOVRING	Ringing Overhead Voltage		VOVRING[14:0][2]															Init	0000	0	V
12	VRING	Scaled RING Voltage Measurement	VRING[15:0]																Diag			V
20	VRNGNG	External Ringing Generator Voltage Measurement		VRNGNG[14:7][3]															Diag			V
11	VTIP	Scaled TIP Voltage Measurement	VTIP[15:0]																Diag			V

Notes:

1. RAM values are 2's complement unless otherwise noted. Any register not listed is reserved and must not be written.
2. Only positive input values are valid for these RAM addresses.
3. Si3225 only.
4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location (RINGFRHI[14:0]) stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.
8. For the Si3225, RINGPHAS[15:0], see description.
9. Silicon Laboratories recommends using the power sum mode when using the Si3200. Please refer to the initialization procedure for information on configuring the therm register to this mode. In this mode, PTH12 and PLPF12 represent the entire power dissipated, and PTH34/56 and PLPF 34/56 are unused. The values above represent the power sum mode.

16-Bit Control Descriptions

BATHTH: High Battery Switch Threshold (RAM Address 31)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		BATHTH[7:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:7	BATHTH[7:0]	**High Battery Switch Threshold.** Programs the voltage threshold for selecting the high battery supply (VBATH). The threshold is compared to the voltage of the most negative lead (when in forward active). 0 to 160.173 V range, 628 mV/LSB, LSB = bit 7.

BATLPF: Battery Tracking Filter Coefficient (RAM Address 34)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	BATLPF[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	BATLPF[12:0]	**Battery Tracking Filter Coefficient.** Programs the digital low-pass filter block that filters the voltage measured on the RING lead when battery tracking is enabled.

BATLTH: Low Battery Switch Threshold (RAM Address 32)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		BATLTH[7:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:7	BATLTH[7:0]	**Low Battery Switch Threshold.** Programs the voltage threshold for selecting the low battery supply (VBATL). The threshold is compared to the voltage of the most negative lead (usually ring when in forward active). 0 to 160.173 V range, 628 mV/LSB, LSB = bit 7.

BSWLPF: RING Voltage Filter Coefficient (RAM Address 33)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	BSWLPF[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	BSWLPF[12:0]	**RING Voltage Filter Coefficient.** Programs the digital low-pass filter block that filters the voltage measured on the RING lead used to determine battery switching threshold.

CMHITH: Speedup Upper Threshold (RAM Address 36)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMHITH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	CMHITH[15:0]	**Speedup Upper Threshold.** Programs the upper threshold of V_{TIP} at which speedup mode in enabled. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for V_{BAT} < 63.3 V).

CMLOTH: Speedup Lower Threshold (RAM Address 35)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMLOTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	CMLOTH[15:0]	**Speedup Threshold.** Programs the lower threshold of V_{TIP} at which speedup mode in enabled. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for V_{BAT} < 63.3 V).

DIAGAC: SLIC Diagnostics AC Output (RAM Address 53)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIAGAC[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	DIAGAC[15:0]	**SLIC Diagnostic AC Output.** Provides filtered value that reflects the ac rms value from the output of the monitor ADC. The input to the monitor ADC is selected by the setting in the SDIAG register (Register 13). The DIAGACCO RAM location determines the rms filter coefficient used. This register should be used for frequencies < 300 Hz.

DIAGACCO: SLIC Diagnostics AC Filter Coefficient (RAM Address 54)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIAGACCO[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DIAGACCO[12:0]	**SLIC Diagnostics AC Filter Coefficient.** Programs the rms filter coefficient used in the ac measurement result from the monitor ADC.

DIAGDC: SLIC Diagnostics DC Output (RAM Address 51)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIAGDC[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	DIAGDC[15:0]	**SLIC Diagnostic DC Output.** Provides a low-pass filtered value that reflects the dc value from the output of the monitor ADC. The input to the monitor ADC is selected by the setting in the SDIAG register (Register 13). The DIAGDCCO RAM location determines the low-pass filter coefficient used.

DIAGDCCO: SLIC Diagnostics DC Filter Coefficient (RAM Address 52)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIAGDCCO[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DIAGDCCO[12:0]	**SLIC Diagnostics DC Filter Coefficient.** Programs the low-pass filter coefficient used in the dc measurement result from the monitor ADC.

DIAGPK: SLIC Diagnostics Peak Detector (RAM Address 55)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIAGPK[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	DIAGPK[15:0]	**SLIC Diagnostic Peak Detector.** Provides filtered value that reflects the peak amplitude from the output of the monitor ADC. The input to the monitor ADC is selected by the setting in the SDIAG register (Register 13).

DTCOL2HTH: DTMF Column Second Harmonic Threshold (RAM Address 118)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTCOL2HTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTCOL2HTH[12:0]	**DTMF Column Second Harmonic Threshold.** Programs the threshold for the power ratio of peak column tone to its second harmonic.

DTCOLRTH: DTMF Column Ratio Threshold (RAM Address 116)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTCOLRTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTCOLRTH[12:0]	**DTMF Column Ratio Threshold.** Programs the threshold for the power ratio of highest power column to the other columns.

DTCOLTH: DTMF Column Peak Threshold (RAM Address 112)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTCOLTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTCOLTH[12:0]	**DTMF Column Peak Threshold.** Programs the minimum power threshold for column DTMF detection. All columns use the same threshold. If the ratio of power in a particular column to total power in the column band exceeds COLTH, then a column detect for that particular column signal is detected.

DTFTWTH: DTMF Forward Twist Threshold (RAM Address 113)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTFTWTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTFTWTH[12:0]	**DTMF Forward Twist Threshold.** Programs the threshold for the power ratio of row power to column power.

DTHOTTH: DTMF Hot Limit Threshold (RAM Address 120)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTHOTTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	DTHOTTH[15:0]	**DTMF Hot Limit Threshold.** Programs the two-step AGC in the DTMF detection path.

DTMINPTH: DTMF Minimum Power Threshold (RAM Address 119)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTMINPTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	DTMINPTH[15:0]	**DTMF Minimum Power Threshold.** Programs the threshold for the minimum total power in the DTMF calculation, under which the calculation is ignored.

DTROW0TH: DTMF Row 0 Peak Threshold (RAM Address 108)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROW0TH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROW0TH[12:0]	**DTMF Row 0 Peak Threshold.** Programs the minimum power threshold for row 0 DTMF detection. If the ratio of power in row 0 to total power in the row band exceeds ROW0TH, then a row 0 signal is detected.

DTROW1TH: DTMF Row 1 Peak Threshold (RAM Address 109)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROW1TH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROW1TH[12:0]	**DTMF Row 1 Peak Threshold.** Programs the minimum power threshold for row 1 DTMF detection. If the ratio of power in row 1 to total power in the row band exceeds ROW1TH, then a row 1 signal is detected.

DTROW2HTH: DTMF Row Second Harmonic Threshold (RAM Address 117)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROW2HTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROW2HTH[12:0]	**DTMF Row Second Harmonic Threshold.** Programs the threshold for the power ratio of peak row tone to its second harmonic.

DTROW2TH: DTMF Row 2 Peak Threshold (RAM Address 110)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROW2TH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROW2TH[12:0]	**DTMF Row 2 Peak Threshold.** Programs the minimum power threshold for row 2 DTMF detection. If the ratio of power in row 2 to total power in the row band exceeds ROW2TH, then a row 2 signal is detected.

DTROW3TH: DTMF Row 3 Peak Threshold (RAM Address 111)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROW3TH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROW3TH[12:0]	**DTMF Row 3 Peak Threshold.** Programs the minimum power threshold for row 3 DTMF detection. If the ratio of power in row 3 to total power in the row band exceeds ROW3TH, then a row 3 signal is detected.

DTROWRTH: DTMF Row Ratio Threshold (RAM Address 115)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTROWRTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTROWRTH[12:0]	**DTMF Row Ratio Threshold.** Programs the threshold for the power ratio of highest power row to the other rows.

DTRTWTH: DTMF Reverse Twist Threshold (RAM Address 114)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTRTWTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	DTRTWTH[12:0]	**DTMF Reverse Twist Threshold.** Programs the threshold for the power ratio of column power to row power.

ECCO0: Echo Cancellation Filter Coefficient 0 (RAM Address 89)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO0[12:0]	**Echo Cancellation Filter Coefficient 0.** Programs the eighth tap of the 8-tap FIR transhybrid balance network filter.

ECCO1: Echo Cancellation Filter Coefficient 1 (RAM Address 82)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO1[12:0]	**Echo Cancellation Filter Coefficient 1.** Programs the first tap of the 8-tap FIR transhybrid balance network filter.

ECCO2: Echo Cancellation Filter Coefficient 2 (RAM Address 83)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO2[12:0]	**Echo Cancellation Filter Coefficient 2.** Programs the second tap of the 8-tap FIR transhybrid balance network filter.

ECCO3: Echo Cancellation Filter Coefficient 3 (RAM Address 84)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO3[12:0]	**Echo Cancellation Filter Coefficient 3.** Programs the third tap of the 8-tap FIR transhybrid balance network filter.

ECCO4: Echo Cancellation Filter Coefficient 4 (RAM Address 85)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO4[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO4[12:0]	**Echo Cancellation Filter Coefficient 4.** Programs the fourth tap of the 8-tap FIR transhybrid balance network filter.

ECCO5: Echo Cancellation Filter Coefficient 5 (RAM Address 86)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO5[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO5[12:0]	**Echo Cancellation Filter Coefficient 5.** Programs the fifth tap of the 8-tap FIR transhybrid balance network filter.

ECCO6: Echo Cancellation Filter Coefficient 6 (RAM Address 87)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO6[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO6[12:0]	**Echo Cancellation Filter Coefficient 6.** Programs the sixth tap of the 8-tap FIR transhybrid balance network filter.

ECCO7: Echo Cancellation Filter Coefficient 7 (RAM Address 88)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECCO7[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECCO7[12:0]	**Echo Cancellation Filter Coefficient 7.** Programs the seventh tap of the 8-tap FIR transhybrid balance network filter.

ECIIRA1: Echo Cancellation IIR Filter Coefficient A1 (RAM Address 92)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECIIRA1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECIIRA1[12:0]	**Echo Cancellation IIR Filter Coefficient A1.** Programs the A1 coefficient of the second-order IIR filter.

ECIIRA2: Echo Cancellation IIR Filter Coefficient A2 (RAM Address 93)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECIIRA2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECIIRA2[12:0]	**Echo Cancellation IIR Filter Coefficient A2.** Programs the A2 coefficient of the second-order IIR filter.

ECIIRB0: Echo Cancellation IIR Filter Coefficient B0 (RAM Address 90)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECIIRB0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECIIRB0[12:0]	**Echo Cancellation IIR Filter Coefficient B0.** Programs the B0 coefficient of the second-order IIR filter.

ECIIRB1: Echo Cancellation IIR Filter Coefficient B1 (RAM Address 91)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECIIRB1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	ECIIRB1[12:0]	**Echo Cancellation IIR Filter Coefficient B1.** Programs the B1 coefficient of the second-order IIR filter.

FSKAMP0: FSK Amplitude for Space (RAM Address 102)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKAMP0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSKAMP0[12:0]	**FSK Amplitude for Space.** Programs the amplitude to be used when generating a space or 0. When the active timer (OSC1T1) expires, the value of this register is loaded into oscillator 1.

FSKAMP1: FSK Amplitude for Mark (RAM Address 103)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKAMP1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSKAMP1[12:0]	**FSK Amplitude for Mark.** Programs the amplitude to be used when generating a mark or 1. When the active timer (OSC1T1) expires, the value of this register is loaded into oscillator 1.

FSKFREQ0: FSK Frequency for Space (RAM Address 100)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKFREQ0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSKFREQ0[12:0]	**FSK Frequency for Space.** Programs the frequency to be used when generating a space or 0. When the active timer (OSC1T1) expires, the value of this register is loaded into oscillator 1.

FSKFREQ1: FSK Frequency for Mark (RAM Address 101)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKFREQ1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSKFREQ1[12:0]	**FSK Frequency for Mark.** Programs the frequency to be used when generating a mark or 1. When the active timer (OSC1T1) expires, the value of this register is loaded into oscillator 1.

FSK01HI: FSK 0-1 Transition Frequency—High Byte (RAM Address 104)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSK01HI[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSK01HI[12:0]	**FSK 0-1 Transition Frequency—High Byte.** Contains the upper byte of a gain correction factor applied to the FSK signal amplitude when transitioning from a space (0) to a mark (1).

FSK01LO: FSK 0-1 Transition Frequency—Low Byte (RAM Address 105)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSK01LO[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSK01LO[12:0]	**FSK 0-1 Transition Frequency—Low Byte.** Contains the lower byte of a gain correction factor applied to the FSK signal amplitude when transitioning from a space (0) to a mark (1).

FSK10HI: FSK1-0 Transition Frequency—High Byte (RAM Address 106)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSK10HI[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSK10HI[12:0]	**FSK 1-0 Transition Frequency—High Byte.** Contains the upper byte of a gain correction factor applied to the FSK signal amplitude when transitioning from a mark (1) to a space (0).

FSK10L0: FSK 1-0 Transition Frequency—Low Byte (RAM Address 107)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FSKT10LO[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	FSKT10LO[12:0]	**FSK 1-0 Transition Frequency—Low Byte.** Contains the lower byte of a gain correction factor applied to the FSK signal amplitude when transitioning from a mark (1) to a space (0).

ILONG: Longitudinal Current Sense Value (RAM Address 9)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ILONG[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	ILONG[15:0]	**Longitudinal Current Sense Value.** Holds the realtime measured longitudinal current. 0 to 101.09 mA measurement range, 3.097 μA/LSB, 500 μA effective resolution (500 μA effective resolution for ILONG < 50.54 mA). Updated at an 800 Hz rate, signed/magnitude.

ILOOP: Loop Current Sense Value (RAM Address 8)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ILOOP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	ILOOP[15:0]	**Loop Current Sense Value.** Holds the realtime measured loop current. 0 to 101.09 mA measurement range, 3.097 μA/LSB, 500 μA effective resolution (250 μA effective resolution for ILOOP < 50.54 mA). Updated at an 800 Hz rate, signed/magnitude.

IRING: (Transistor Q5) Current Measurement (RAM Address 18)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IRING[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	IRING[15:0]	**IRING (Transistor Q5) Current Measurement.** Reflects the current flowing into the IRING pin of the Si3200 (transistor Q5 of a discrete circuit). 3.097 μA/LSB, 2's complement.

IRINGN: (Transistor Q3) Current Measurement (RAM Address 16)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IRINGN[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	IRINGN[15:0]	**IRINGN (Transistor Q3) Current Measurement.** Reflects the current flowing into the IRINGN pin of the Si3200 (transistor Q3 of a discrete circuit). 195.3 nA/LSB, 2's complement. Effective resolution of 10 μA for Si3200 and 25 μA for discretes.

IRINGP: (Transistor Q2) Current Measurement (RAM Address 15)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IRINGP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	IRINGP[15:0]	**IRINGP (Transistor Q2) Current Measurement.** Reflects the current flowing into the IRINGP pin of the Si3200 (transistor Q2 of a discrete circuit). 3.097 μA/LSB, 2's complement. Effective resolution of 198.2 μA. Effective resolution of 396.4 μA for I_{LOOP} > 50 mA

IRNGNG: External Ringing Generator Current Measurement (RAM Address 21)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IRNGNG[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	IRNGNG[15:0]	**External Ringing Generator Current Measurement.** Reflects the current generated by the external ringing generator. This location is only available on the Si3225. 10,156/R_{RNGNG} μA/LSB, 2's complement. Effective resolution of 1.3 V/R_{RNGNG} A/LSB.

ITIP: (Transistor Q6) Current Measurement (RAM Address 19)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ITIP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	ITIP[15:0]	**ITIP (Transistor Q6) Current Measurement.** Reflects the current flowing into the ITIP pin of the Si3200 (transistor Q6 of a discrete circuit). 3.097 μA/LSB, 2's complement.

ITIPN: (Transistor Q4) Current Measurement (RAM Address 17)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ITIPN[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	ITIPN[15:0]	**ITIPN (Transistor Q4) Current Measurement.** Reflects the current flowing into the ITIPN pin of the Si3200 (transistor Q4 of a discrete circuit). 195.3 nA/LSB, 2's complement. Effective resolution of 10 μA for Si3200 and 25 μA for discretes.

ITIPP: (Transistor Q1) Current Measurement (RAM Address 14)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ITIPP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	ITIPP[15:0]	**ITIPP (Transistor Q1) Current Measurement.** Reflects the current flowing into the ITIPP pin of the Si3200 (transistor Q1 of a discrete circuit). 3.097 μA/LSB, 2's complement. Effective resolution of 198.21 μA. Effective resolution of 396.4 μA for I_{loop} > 50 mA.

LCRDBI: Loop Closure Detection Debounce Interval (RAM Address 24)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCRDBI[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LCRDBI[15:0]	**Loop Closure Detection Debounce Interval.** Programs the debounce interval during the loop closure detection process. Programmable range is 0 to 40.96 s at 1.25 ms/LSB.

LCRLPF: Loop Closure Filter Coefficient (RAM Address 25)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCRLPF[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	LCRLPF[12:0]	**Loop Closure Filter Coefficient.** Programs the digital low-pass filter block in the loop closure detection circuit. Refer to data sheet for calculation.

LCRMASK: Loop Closure Mask Interval Coefficient (RAM Address 26)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCRMASK[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LCRMASK[15:0]	**Loop Closure Mask Interval Coefficient.** Programs the loop closure detection mask interval. Programmable range is 0 to 40.96 s at 1.25 ms/LSB.

LCRMSKPR: LCR Mask During Polarity Reversal (RAM Address 166)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCRMSKPR[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LCRMSKPR[15:0]	**LCR Mask During Polarity Reversal.** Programs the loop closure detection mask interval during a polarity reversal. Programmable range is 0 to 40.96 s at 1.25 ms/LSB.

LCROFFHK: Loop Closure Detection Threshold—On-Hook to Off-Hook Transition (RAM Address 22)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCROFFHK[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LCROFFHK[15:0]	**Loop Closure Detection Threshold—On-Hook to Off-Hook Transition.** Programs the loop current threshold at which a valid loop closure is detected when transitioning from on-hook to off-hook. Hysteresis is provided by programming the LCRONHK RAM location to a different value that detects the off-hook to on-hook transition threshold. 0 to 101.09 mA programmable range, 3.097 μA/LSB, 396.4 μA effective resolution. Usable range is 0 to 61 mA.

LCRONHK: Loop Closure Detection Threshold—Off-Hook to On-Hook Transition (RAM Address 23)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCRONHK[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LCRONHK[15:0]	**Loop Closure Detection Threshold—Off-Hook to On-Hook Transition.** Programs the loop current threshold at which a valid loop closure event has been terminated (the off-hook to on-hook transition). LCRONHK provides hysteresis to a loop closure event when set approximately 1 mA lower than the LCROFFHK threshold. 0 to 101.09 mA programmable range, 3.097 μA/LSB, 396.4 μA effective resolution. Usable range is 0 to 61 mA.

LONGDBI: Ground Key Detection Debounce Interval (RAM Address 29)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LONGDBI[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LONGDBI[15:0]	**Ground Key Detection Debounce Interval.** Programs the debounce interval during the ground key detection process. Programmable range is 0 to 40.96 s at 1.25 ms/LSB.

LONGHITH: Ground Key Detection Threshold (RAM Address 27)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LONGHITH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LONGHITH[15:0]	**Ground Key Detection Threshold.** Programs the longitudinal current threshold at which a valid ground key event is detected. Hysteresis is provided by programming the LONGLOTH RAM location to a different value that detects the removal of a ground key event. 0 to 101.09 mA programmable range, 3.097 μA/LSB, 396.4 μA effective resolution. Usable range is 0 to 16 mA.

LONGLOTH: Ground Key Removal Detection Threshold (RAM Address 28)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LONGLOTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	LONGLOTH[15:0]	**Ground Key Removal Detection Threshold.** Programs the longitudinal current threshold at which it is determined that a ground key event has been terminated. 0 to 101.09 mA programmable range, 3.097 μA/LSB, 396.4 μA effective resolution. Usable range is 0 to 16 mA.

LONGLPF: Ground Key Filter Coefficient (RAM Address 30)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LONGLPF[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	LONGLPF[12:0]	**Ground Key Filter Coefficient.** Programs the digital low-pass filter block in the ground key detection circuit. Refer to data sheet for calculation.

OSC1AMP: Oscillator 1 Amplitude (RAM Address 95)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1AMP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	OSC1AMP[15:0]	**Oscillator 1 Amplitude.** Programs tone generator 1 amplitude. Refer to data sheet for use.

OSC1FREQ: Oscillator 1 Frequency (RAM Address 94)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1FREQ[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	OSC1FREQ[12:0]	**Oscillator 1 Frequency.** Programs the frequency of tone generator 1. Refer to data sheet for use.

OSC1PHAS: Oscillator 1 Initial Phase (RAM Address 96)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC1PHAS[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	OSC1PHAS[15:0]	**Oscillator 1 Initial Phase.** Programs the initial phase of tone generator 1.

OSC2AMP: Oscillator 2 Amplitude (RAM Address 98)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2AMP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	OSC2AMP[15:0]	**Oscillator 2 Amplitude.** Programs tone generator 2 amplitude.

OSC2FREQ: Oscillator 2 Frequency (RAM Address 97)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2FREQ[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	OSC2FREQ[12:0]	**Oscillator 2 Frequency.** Programs the frequency of tone generator 2.

OSC2PHAS: Oscillator 2 Initial Phase (RAM Address 99)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSC2PHAS[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	OSC2PHAS[15:0]	**Oscillator 2 Initial Phase.** Programs the initial phase of tone generator 2.

PLPF12: Q1/Q2 Thermal Low-Pass Filter Coefficient (RAM Address 40)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLPF12[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	PLPF12[12:0]	**Q1/Q2 Thermal Low-Pass Filter Coefficient.** Programs the thermal low-pass filter value used to calculate the power in transistors Q1 and Q2. Also used to set thermal LPF when using Si3200. Refer to data sheet for use.

PLPF34: Q3/Q4 Thermal Low-Pass Filter Coefficient (RAM Address 41)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLPF34[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	PLPF34[12:0]	**Q3/Q4 Thermal Low-Pass Filter Coefficient.** Programs the thermal low-pass filter value used to calculate the power in transistors Q3 and Q4. Refer to data sheet for use.

PLPF56: Q5/Q6 Thermal Low-Pass Filter Coefficient (RAM Address 42)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLPF56[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	PLPF56[12:0]	**Q5/Q6 Thermal Low-Pass Filter Coefficient.** Programs the thermal low-pass filter value used to calculate the power in transistors Q5 and Q6. Refer to data sheet for use.

PMAMPL: Pulse Metering Amplitude (RAM Address 68)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMAMPL[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PMAMPL[15:0]	**Pulse Metering Amplitude.** Programs the voltage amplitude of the pulse metering signal. This function is only valid for Si3220. Refer to data sheet for use.

PMAMPTH: Pulse Metering AGC Amplitude Threshold (RAM Address 70)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMAMPTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PMAMPTH[15:0]	**Pulse Metering AGC Amplitude Threshold.** Programs the voltage threshold for the automatic gain control (AGC) stage in the transmit audio path. This function is only valid for Si3220. Refer to data sheet for use.

PMFREQ: Pulse Metering Frequency (RAM Address 67)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMFREQ[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PMFREQ[12:0]	**Pulse Metering Frequency.** Programs the frequency of the pulse metering signal. This function is only valid for Si3220. Refer to data sheet for use.

PMRAMP: Pulse Metering Ramp Rate (RAM Address 69)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMRAMP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PMRAMP[15:0]	**Pulse Metering Ramp Rate.** Programs the attack and decay rate of the pulse metering signal. This function is only valid for Si3220. Programmable range is 0 to 4.096 s at 0.125 ms/LSB (15 bit).

PQ1DH: Q1 Calculated Power (RAM Address 44)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ1DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ1DH[15:0]	**Q1 Calculated Power.** Provides the calculated power in transistor Q1. Used with discrete linefeed circuitry. 0 to 16.319 W range, 498 μW/LSB.

PQ2DH: Q2 Calculated Power (RAM Address 45)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ2DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ2DH[15:0]	**Q2 Calculated Power.** Provides the calculated power in transistor Q2. Used with discrete linefeed circuitry. 0 to 16.319 W range, 498 μW/LSB.

PQ3DH: Q3 Calculated Power (RAM Address 46)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ3DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ3DH[15:0]	**Q3 Calculated Power.** Provides the calculated power in transistor Q3. Used with discrete linefeed circuitry. 0 to 1.03 W range, 31.4 μW/LSB.

PQ4DH: Q4 Calculated Power (RAM Address 47)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ4DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ4DH[15:0]	**Q4 Calculated Power.** Provides the calculated power in transistor Q4. Used with discrete linefeed circuitry. 0 to 1.03 W range, 31.4 μW/LSB.

PQ5DH: Q5 Calculated Power (RAM Address 48)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ5DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ5DH[15:0]	**Q5 Calculated Power.** Provides the calculated power in transistor Q5. Used with discrete linefeed circuitry. 0 to 16.319 W range, 498 μW/LSB.

PQ6DH: Q6 Calculated Power (RAM Address 49)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PQ6DH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PQ6DH[15:0]	**Q6 Calculated Power.** Provides the calculated power in transistor Q6. Used with discrete linefeed circuitry. 0 to 16.319 W range, 498 μW/LSB.

PSUM: Total Calculated Power (RAM Address 50)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PSUM[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PSUM[15:0]	**Total Calculated Power.** Provides the total calculated power in transistors Q1 through Q6. Using the Si3200, this RAM location reflects the total power dissipated in the Si3200 package. 0 to 34.72 W range, 1059.6 μW/LSB.

PTH12: Q1/Q2 Power Alarm Threshold (RAM Address 37)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTH12[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PTH12[15:0]	**Q1/Q2 Power Alarm Threshold.** Programs the power threshold in transistors Q1 and Q2 at which a power alarm is triggered. Also programs the total power threshold when using the Si3200. 0 to 16.319 W programmable range, 498 μW/LSB (0 to 34.72 W range, 1059.6 μW/LSB in Si3200 mode). Refer to data sheet for use.

PTH34: Q3/Q4 Power Alarm Threshold (RAM Address 38)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTH34[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PTH34[15:0]	**Q3/Q4 Power Alarm Threshold.** Programs the power threshold in transistors Q3 and Q4 at which a power alarm is triggered. 0 to 1.03 W programmable range, 31.4 μW/LSB. Refer to data sheet for use.

PTH56: Q5/Q6 Power Alarm Threshold (RAM Address 39)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTH56[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	PTH56[15:0]	**Q5/Q6 Power Alarm Threshold.** Programs the power threshold in transistors Q5 and Q6 at which a power alarm is triggered. 0 to 16.319 W programmable range, 498 μW/LSB. Refer to data sheet for use.

RB56: Q5/Q6 Base Resistance (RAM Address 43)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RB56[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RB56[15:0]	**Q5/Q6 Base Resistance.** Programs the base resistance feeding transistors Q5 and Q6.

RINGAMP: Ringing Amplitude/Zero Crossing Delay (RAM Address 59)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGAMP[15:0]/ZERDELAY[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RINGAMP[15:0]/ ZERDELAY[15:0]	**Ringing Amplitude/Zero Crossing Delay.** For the Si3220, this RAM location programs the peak ringing amplitude. For the Si3225, this RAM location stores the desired delay between the last zero current crossing event and the next opportunity to open the ringing relay. Refer to data sheet for use.

Reset settings = 0x00

RINGFRHI: Ringing Frequency High Byte/Linefeed Status Delay (RAM Address 57)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		RINGFRHI[11:0]/LFSDELAY[11:0]														
Type	R/W															

Bit	Name	Function
14:3	RINGFRHI[11:0]/ LFSDELAY[11:0]	**Ringing Frequency High Byte/Linefeed Status Delay.** For the Si3220, this RAM location programs the upper byte of the ringing frequency coefficient. The RINGFRLO RAM location holds the lower byte. For the Si3225, this RAM location programs the amount of delay between when the ringing relay opens and when the linefeed status (LFS) register transitions out of the ringing state. Refer to data sheet for use.

RINGFRLO: Ringing Frequency Low Byte (RAM Address 58)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		RINGFRLO[11:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:3	RINGFRLO[11:0]	**Ringing Frequency Low Byte.** For the Si3220, this RAM location programs the lower byte of the ringing frequency coefficient. The RINGFRHI RAM location holds the upper byte. For the Si3225, this RAM location is not used. Refer to data sheet for use.

RINGOF: Ringing Waveform DC Offset (RAM Address 56)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		RINGOF[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	RINGOF[14:0]	**Ringing Waveform DC Offset.** Programs the amount of dc offset that is added to the ringing waveform during ringing mode. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution. Refer to data sheet for use.

RINGPHAS: Ringing Oscillator Initial Phase (RAM Address 60)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RINGPHAS[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RINGPHAS[12:0]	**RInging Oscillator Initial Phase.** Programs the initial phase of the ringing oscillator. 0 to 1.024 s range, 31.25 μs/LSB for Si3220 with trapezoidal ringing. For the Si3225, programs zero current cross hysteresis value. (0 to 662.83 mA range, 20.3 μA/LSB, 2.6 μA effective resolution). Used for filtering Ringtrip current measurements.

RTACDB: AC Ring Trip Debounce Interval (RAM Address 66)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTACDB[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTACDB[15:0]	**AC Ring Trip Debounce Interval.** Programs the debounce interval for the ac loop current detection circuit. Refer to the Si3220/25 data sheet for calculation.

RTACTH: AC Ring Trip Detect Threshold (RAM Address 64)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTACTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTACTH[15:0]	**AC Ring Trip Detect Threshold.** Programs the ac loop current threshold value above which a valid ring trip event is detected. See Si3220/Si3225 data sheet for recommended values.

RTCOUNT: Ring Trip Timeout Counter (RAM Address 61)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTCOUNT[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTCOUNT[15:0]	**Ring Trip Timeout Counter.** Programs the timeout value that, when reached, will force the ringing relay to open regardless of whether a zero current crossing has been detected. 125 μs/LSB. See Si3220/Si3225 data sheet for recommended values.

RTDCDB: DC Ring Trip Debounce Interval (RAM Address 65)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTDCDB[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTDCDB[15:0]	**DC Ring Trip Debounce Interval.** Programs the debounce interval for the dc loop current detection circuit. Refer to the Si3220/25 data sheet for calculation

RTDCTH: DC Ring Trip Detect Threshold (RAM Address 62)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTDCTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTDCTH[15:0]	**DC Ring Trip Detect Threshold.** Programs the dc loop current threshold value above which a valid ring trip event is detected. See Si3220/Si3225 data sheet for recommended values.

RTPER: Ring Trip Sample Period (RAM Address 63)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTPER[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RTPER[15:0]	**Ring Trip Sample Period.** Programs the sample period used in the ring trip detection circuit. See Si3220/ Si3225 data sheet for recommended values.

RXIIRPOL: Receive IIR Filter Pole Coefficient (RAM Address 81)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXIIRPOL[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXIIRPOL[12:0]	**Receive IIR Filter Pole Coefficient.** Programs the pole of the receive IIR filter.

RXEQCO0: Receive Equalizer Coefficient 0 (RAM Address 80)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXEQCO0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXEQCO0[12:0]	**Receive Equalizer Coefficient 0.** Programs the one of the four receive equalizer coefficients.

RXEQCO1: Receive Equalizer Coefficient 1 (RAM Address 79)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXEQCO1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXEQCO1[12:0]	**Receive Equalizer Coefficient 1.** Programs the one of the four receive equalizer coefficients.

RXEQCO2: Receive Equalizer Coefficient 2 (RAM Address 78)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXEQCO2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXEQCO2[12:0]	**Receive Equalizer Coefficient 2.** Programs the one of the four receive equalizer coefficients.

RXEQCO3: Receive Equalizer Coefficient 3 (RAM Address 77)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXEQCO3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXEQCO3[12:0]	**Receive Equalizer Coefficient 3.** Programs the one of the four receive equalizer coefficients.

RXGAIN: Receive Gain Control (RAM Address 71)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXGAIN[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXGAIN[12:0]	**Receive Gain Control.** Programs the gain/attenuation for the receive path. The digital signal is effectively multiplied by RXGAIN to achieve gain/attenuation. RXGAIN is a 12-bit linear, 0 to 2, gain block. A value of 0x00 corresponds to –∞ dB gain (mute). A value of 0x4000 corresponds to unity gain. A value of 0x7FF8 corresponds to a gain of 6 dB.

RXMODPWR: Receive Path Modem Tone Power (RAM Address 123)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXMODPWR[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	RXMODPWR[12:0]	**Receive Path Modem Tone Power.** Reports the receive path signal power of the 2100 Hz modem initialization tone.

RXPWR: Receive Path Input Signal Power (RAM Address 121)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXPWR[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	RXPWR[15:0]	**Receive Path Input Signal Power.** Reports the total power of the receive path input signal.

SPEEDUP: DC Settling Speedup Timer (RAM Address 168)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SPEEDUP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	SPEEDUP[15:0]	**DC Settling Speedup Timer.** Programs the dc speedup timer that allows quicker settling during loop transitions. This timer is invoked by the common mode threshold detectors (CMHITH and CMLOTH). 1.25 ms/LSB, exception: 0x0000 = 60 ms (default).

SPEEDUPR: DC Settling Speedup Timer after Ringing (RAM Address 169)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SPEEDUPR[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	SPEEDUPR[15:0]	**DC Settling Speedup Timer for Ringing.** Programs the dc speedup timer that allows quicker settling following a Ringing burst. This timer is invoked by any mode change from the Ring state. 1.25 ms/LSB, exception: 0x0000 = 60 ms (default). 40.96 s range.

TESTA1H1: Transmit Path Diagnostics Filter 1 Coefficient A1—High Byte (RAM Address 132)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1H1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1H1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient A1—High Byte.** Programs the upper 13 bits of the A1 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTA1H2: Transmit Path Diagnostics Filter 2 Coefficient A1—High Byte (RAM Address 142)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1H2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1H2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient A1—High Byte.** Programs the upper 13 bits of the A1 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTA1H3: Transmit Path Diagnostics Filter 3 Coefficient A1—High Byte (RAM Address 152)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1H3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1H3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient A1—High Byte.** Programs the upper 13 bits of the A1 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTA1L1: Transmit Path Diagnostics Filter 1 Coefficient A1—Low Byte (RAM Address 131)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1L1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1L1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient A1—Low Byte.** Programs the lower 13 bits of the A1 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTA1L2: Transmit Path Diagnostics Filter 2 Coefficient A1—Low Byte (RAM Address 141)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1L2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1L2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient A1—Low Byte.** Programs the lower 13 bits of the A1 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTA1L3: Transmit Path Diagnostics Filter 3 Coefficient A1—Low Byte (RAM Address 151)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA1L3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA1L3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient A1—Low Byte.** Programs the lower 13 bits of the A1 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTA2H1: Transmit Path Diagnostics Filter 1 Coefficient A2—High Byte (RAM Address 134)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2H1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2H1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient A2—High Byte.** Programs the upper 13 bits of the A2 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTA2H2: Transmit Path Diagnostics Filter 2 Coefficient A2—High Byte (RAM Address 144)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2H2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2H2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient A2—High Byte.** Programs the upper 13 bits of the A2 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTA2H3: Transmit Path Diagnostics Filter 3 Coefficient A2—High Byte (RAM Address 154)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2H3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2H3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient A2—High Byte.** Programs the upper 13 bits of the A2 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTA2L1: Transmit Path Diagnostics Filter 1 Coefficient A2—Low Byte (RAM Address 133)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2L1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2L1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient A2—Low Byte.** Programs the lower 13 bits of the A2 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTA2L2: Transmit Path Diagnostics Filter 2 Coefficient A2—Low Byte (RAM Address 143)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2L2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2L2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient A2—Low Byte.** Programs the lower 13 bits of the A2 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTA2L3: Transmit Path Diagnostics Filter 3 Coefficient A2—Low Byte (RAM Address 153)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTA2L3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTA2L3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient A2—Low Byte.** Programs the lower 13 bits of the A2 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTAVO: Transmit Path Diagnostics Filter Average Output (RAM Address 156)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTAVO[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	TESTAVO[15:0]	**Transmit Path Diagnostics Filter Average Output.** Reflects the average output of the transmit path diagnostics filters, updated at the end of each window defined by the TESTWLN RAM location.

TESTAVBW: Transmit Path Diagnostics Filter Average Bandwidth (RAM Address 158)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTAVBW[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTAVBW[12:0]	**Transmit Path Diagnostics Filter Average Bandwidth.** Programs the bandwidth to be used when determining the average output measurement stored in the TESTAVO RAM location.

TESTAVFL: Transmit Path Diagnostics Filter Average Flag (RAM Address 160)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTAVFL[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTAVFL[12:0]	**Transmit Path Diagnostics Filter Peak Flag.** Represents a flag that signals the average power is higher than the average power threshold RAM location (TESTAVTH).

TESTAVTH: Transmit Path Diagnostics Filter Average Threshold (RAM Address 162)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTAVTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTAVTH[12:0]	**Transmit Path Diagnostics Filter Average Threshold.** Programs the average power threshold that will trip the TESTAVFL flag in RAM location 160.

TESTB0H1: Transmit Path Diagnostics Filter 1 Coefficient B0—High Byte (RAM Address 126)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0H1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0H1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B0—High Byte.** Programs the upper 13 bits of the B0 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB0H2: Transmit Path Diagnostics Filter 2 Coefficient B0—High Byte (RAM Address 136)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0H2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0H2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B0—High Byte.** Programs the upper 13 bits of the B0 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB0H3: Transmit Path Diagnostics Filter 3 Coefficient B0—High Byte (RAM Address 146)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0H3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0H3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B0—High Byte.** Programs the upper 13 bits of the B0 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTB0L1: Transmit Path Diagnostics Filter 1 Coefficient B0—Low Byte (RAM Address 125)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0L1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0L1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B0—Low Byte.** Programs the lower 13 bits of the B0 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB0L2: Transmit Path Diagnostics Filter 2 Coefficient B0—Low Byte (RAM Address 135)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0L2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0L2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B0—Low Byte.** Programs the lower 13 bits of the B0 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB0L3: Transmit Path Diagnostics Filter 3 Coefficient B0—Low Byte (RAM Address 145)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB0L3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB0L3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B0—Low Byte.** Programs the lower 13 bits of the B0 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTB1H1: Transmit Path Diagnostics Filter 1 Coefficient B1—High Byte (RAM Address 128)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1H1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1H1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B1—High Byte.** Programs the upper 13 bits of the B1 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB1H2: Transmit Path Diagnostics Filter 2 Coefficient B1—High Byte (RAM Address 138)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1H2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1H2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B1—High Byte.** Programs the upper 13 bits of the B1 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB1H3: Transmit Path Diagnostics Filter 3 Coefficient B1—High Byte (RAM Address 148)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1H3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1H3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B1—High Byte.** Programs the upper 13 bits of the B1 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTB1L1: Transmit Path Diagnostics Filter 1 Coefficient B1—Low Byte (RAM Address 127)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1L1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1L1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B1—Low Byte.** Programs the lower 13 bits of the B1 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB1L2: Transmit Path Diagnostics Filter 2 Coefficient B1—Low Byte (RAM Address 137)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1L2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1L2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B1—Low Byte.** Programs the lower 13 bits of the B1 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB1L3: Transmit Path Diagnostics Filter 3 Coefficient B1—Low Byte (RAM Address 147)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB1L3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB1L3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B1—Low Byte.** Programs the lower 13 bits of the B1 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTB2H1: Transmit Path Diagnostics Filter 1 Coefficient B2—High Byte (RAM Address 130)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2H1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2H1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B2—High Byte.** Programs the upper 13 bits of the B2 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB2H2: Transmit Path Diagnostics Filter 2 Coefficient B2—High Byte (RAM Address 140)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2H2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2H2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B2—High Byte.** Programs the upper 13 bits of the B2 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB2H3: Transmit Path Diagnostics Filter 3 Coefficient B2—High Byte (RAM Address 150)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2H3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2H3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B2—High Byte.** Programs the upper 13 bits of the B2 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTB2L1: Transmit Path Diagnostics Filter 1 Coefficient B2—Low Byte (RAM Address 129)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2L1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2L1[12:0]	**Transmit Path Diagnostics Filter 1 Coefficient B2—Low Byte.** Programs the lower 13 bits of the B2 coefficient in the first second-order IIR transmit path diagnostics filter.

TESTB2L2: Transmit Path Diagnostics Filter 2 Coefficient B2—Low Byte (RAM Address 139)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2L2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2L2[12:0]	**Transmit Path Diagnostics Filter 2 Coefficient B2—Low Byte.** Programs the lower 13 bits of the B2 coefficient in the second second-order IIR transmit path diagnostics filter.

TESTB2L3: Transmit Path Diagnostics Filter 3 Coefficient B2—Low Byte (RAM Address 149)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTB2L3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTB2L3[12:0]	**Transmit Path Diagnostics Filter 3 Coefficient B2—Low Byte.** Programs the lower 13 bits of the B2 coefficient in the third second-order IIR transmit path diagnostics filter.

TESTPKFL: Transmit Path Diagnostics Filter Peak Flag (RAM Address 159)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTPKFL[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTPKFL[12:0]	**Transmit Path Diagnostics Filter Peak Flag.** Represents a flag that signals the peak power is higher than the peak power threshold RAM location (TESTPKTH).

TESTPKO: Transmit Path Diagnostics Filter Peak Output (RAM Address 155)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTPKO[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTPKO[12:0]	**Transmit Path Diagnostics Filter Peak Output.** Reflects the peak output of the transmit path diagnostics filters, updated at the end of each window defined by the TESTWLN RAM location.

TESTPKTH: Transmit Path Diagnostics Filter Peak Threshold (RAM Address 161)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTPKTH[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTPKTH[12:0]	**Transmit Path Diagnostics Filter Peak Flag.** Programs the peak power threshold that will trip the TESTPKFL flag in RAM location 159.

TESTWLN: Transmit Path Diagnostics Filter Window Length (RAM Address 157)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TESTWLN[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TESTWLN[12:0]	**Transmit Path Diagnostics Filter Window Length.** Programs the window length used for the peak output measurement stored in the TESTPKO RAM location.

TXEQCO0: Transmit Equalizer Coefficient 0 (RAM Address 76)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXEQCO0[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXEQCO0[12:0]	**Transmit Equalizer Coefficient 0.** Programs the one of the four transmit equalizer coefficients.

TXEQCO1: Transmit Equalizer Coefficient 1 (RAM Address 75)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXEQCO1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXEQCO1[12:0]	**Transmit Equalizer Coefficient 1.** Programs the one of the four transmit equalizer coefficients.

TXEQCO2: Transmit Equalizer Coefficient 2 (RAM Address 74)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXEQCO2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXEQCO2[12:0]	**Transmit Equalizer Coefficient 2.** Programs the one of the four transmit equalizer coefficients.

TXEQCO3: Transmit Equalizer Coefficient 3 (RAM Address 73)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXEQCO3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXEQCO3[12:0]	**Transmit Equalizer Coefficient 3.** Programs the one of the four transmit equalizer coefficients.

TXGAIN: Transmit Gain Control (RAM Address 72)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXGAIN[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXGAIN[12:0]	**Transmit Gain Control.** Programs the gain/attenuation for the transmit path. The digital signal is effectively multiplied by TXGAIN to achieve gain/attenuation. TXGAIN is a 12-bit linear, 0 to 2, gain block. A value of 0x00 corresponds to –∞ dB gain (mute). A value of 0x4000 corresponds to unity gain. A value of 0x7FF8 corresponds to a gain of 6 dB.

TXHPF1: Transmit High Pass Filter Coefficient 1 (RAM Address 163)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXHPF1[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXHPF1[12:0]	**Transmit High Pass Filter Coefficient 1.** Programs the first transmit high pass filter coefficient.

TXHPF2: Transmit High Pass Filter Coefficient 2 (RAM Address 164)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXHPF2[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXHPF2[12:0]	**Transmit High Pass Filter Coefficient 2.** Programs the second transmit high pass filter coefficient.

TXHPF3: Transmit High Pass Filter Coefficient 3 (RAM Address 165)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXHPF3[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXHPF3[12:0]	**Transmit High Pass Filter Coefficient 3.** Programs the third transmit high pass filter coefficient.

TXMODPWR: Transmit Path Modem Tone Power (RAM Address 124)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXMODPWR[12:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:3	TXMODPWR[12:0]	**Transmit Path Modem Tone Power.** Reports the transmit path signal power of the 2100 Hz modem initialization tone.

TXPWR: Transmit Path Input Signal Power (RAM Address 122)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXPWR[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	TXPWR[15:0]	**Transmit Path Input Signal Power.** Reports the total power of the transmit path input signal.

VBAT: Scaled Battery Voltage Measurement (RAM Address 13)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VBAT[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VBAT[15:0]	**Scaled Battery Voltage Measurement.** Reflects the battery voltage measured through the monitor ADC. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for VBAT < 63.3 V).

VCM: Common Mode Voltage (RAM Address 4)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VCM[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	VCM[14:0]	**Common Mode Voltage.** Programs the common mode voltage between the TIP lead and ground in normal polarity (between RING and ground in reverse polarity). The recommended default value is 3 V, but can be programmed between 0 and 63.3 V. 4.907 mV/LSB, 1.005 V effective resolution.

VLOOP: Loop Voltage Sense Value (RAM Address 7)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VLOOP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VLOOP[15:0]	**Loop Voltage Sense Value.** Holds the realtime measured loop voltage across TIP-RING. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for VLOOP < 64.07 V). Updated at an 800 Hz rate, signed/magnitude.

VOC: Open Circuit Voltage (RAM Address 0)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VOC[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	VOC[14:0]	**Open Circuit Voltage.** Programs the TIP-RING voltage during on-hook conditions. The recommended default value is 48 V but can be programmed between 0 and 63.3 V. 4.907 mV/LSB, 1.005 V effective resolution.

VOCDELTA: Open Circuit Off-Hook Offset Voltage (RAM Address 1)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VOCDELTA[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	VOCDELTA[14:0]	**Open Circuit Off-Hook Offset Voltage.** Programs the amount of offset that is added to the VOC RAM value when the device transitions to off-hook. The recommended default value is 7 V. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VOCHTH: V_{OC} Delta Upper Threshold (RAM Address 3)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VOCHTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VOCHTH[15:0]	**V_{OC} Delta Upper Threshold.** Programs the voltage delta above the VOC value at which the VOCDELTA offset voltage is removed. This threshold is only applicable during the off-hook to on-hook transition, and the VOCTHDL RAM location determines the threshold voltage during the on-hook to off-hook transition. Default value is 2 V. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VOCLTH: V_{OC} Delta Lower Threshold (RAM Address 2)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VOCLTH[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VOCLTH[15:0]	**V_{OC} Delta Lower Threshold.** Programs the voltage delta below the VOC value at which the VOCDELTA offset voltage is added. This threshold is only applicable during the on-hook to off-hook transition, and the VOCTHDH RAM location determines the threshold voltage during the off-hook to on-hook transition. Default value is –8 V. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VOCTRACK: Battery Tracking Open Circuit Voltage (RAM Address 10)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VOCTRACK[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VOCTRACK[15:0]	**Battery Tracking Open Circuit Voltage.** Reflects the TIP-RING voltage during on-hook conditions when the battery supply has dropped below the point where the VOC setting cannot be maintained. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VOV: Overhead Voltage (RAM Address 5)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VOV[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	VOV[14:0]	**Overhead Voltage.** Programs the overhead voltage between the RING lead and the voltage on the VBAT pin in normal polarity (between TIP and ground in reverse polarity). This value will increase or decrease as the battery voltage changes to maintain a constant open circuit voltage, but will maintain its user-defined setting to ensure sufficient overhead for audio transmission when the battery voltage decreases. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VOVRING: Ringing Overhead Voltage (RAM Address 6)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VOVRING[14:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:0	VOVRING[14:0]	**Ringing Overhead Voltage.** Programs the overhead voltage between the peak negative ringing level and VBATH. This value increases or decreases as the battery voltage changes in order to maintain a constant open circuit voltage, but maintains its user-defined setting to ensure sufficient overhead for audio transmission when the battery voltage decreases. 0 to 63.3 V programmable range, 4.907 mV/LSB, 1.005 V effective resolution.

VRING: Scaled RING Voltage Measurement (RAM Address 12)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VRING[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VRING[15:0]	**Scaled RING Voltage Measurement.** Reflects the RING to ground voltage measured through the monitor ADC. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for VRING < 64.07 V). Updated at 800 Hz rate 2's complement.

VRNGNG: External Ringing Generator Voltage Measurement (RAM Address 20)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		VRNGNG[7:0]														
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
14:7	VRNGNG[7:0]	**External Ringing Generator Voltage Measurement.** Reflects the voltage generated by the external ringing generator. This location is only available on the Si3225. 0 to 332.04 V range, 10.172 mV/LSB, 2's complement, LSB = bit 7. (1.302 V effective resolution)

VTIP: Scaled TIP Voltage Measurement (RAM Address 11)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VTIP[15:0]															
Type	R/W															

Reset settings = 0x00

Bit	Name	Function
15:0	VTIP[15:0]	**Scaled TIP Voltage Measurement.** Reflects the TIP to ground voltage measured through the monitor ADC. 0 to 160.173 V range, 4.907 mV/LSB, 628 mV effective resolution (251 mV effective resolution for VTIP < 64.07 V). Updated at an 800 Hz rate, 2's complement.

Document Change List

Revision 0.9 to Revision 0.95

- "RAM Access by Pipeline," on page 1 updated.
- "Protected Register Bits," on page 2 updated.
- "Dual ProSLIC Initialization," on page 2 added.
- "Dual ProSLIC Calibration," on page 2 added.
- Table 1 on page 3 added.
- Table 2 on page 5 added.
- "8-Bit Control Register Summary[1,2]," on page 7 updated.
- "ID: Chip Identification (Register Address 0)," on page 16 updated.
- "PCMMODE: PCM Mode Select (Register Address 53)," on page 33 updated.
- "RAMSTAT: RAM Address Status (Register Address 4)," on page 40 updated.
- "RINGCON: Ringing Configuration (Register Address 23)," on page 41 updated.
- "RLYCON: Relay Driver and Battery Switching Configuration (Register Address 5)," on page 44 updated.
- "SBIAS: SLIC Bias Control (Register Address 8)," on page 45 updated.
- "ZA2HI: Impedance Synthesis Coefficient A2—High Byte (Register Address 52)," on page 50 updated.
- "THERM: Si3200 Thermometer (Register Address 72)," on page 46 updated.
- "Internal 16-Bit RAM Summary[1]," on page 57 updated.
- "PQ1DH: Q1 Calculated Power (RAM Address 44)," on page 88 updated.
- "PQ2DH: Q2 Calculated Power (RAM Address 45)," on page 88 updated.
- "PQ3DH: Q3 Calculated Power (RAM Address 46)," on page 89 updated.
- "PQ4DH: Q4 Calculated Power (RAM Address 47)," on page 89 updated.
- "PQ5DH: Q5 Calculated Power (RAM Address 48)," on page 89 updated.
- "PQ6DH: Q6 Calculated Power (RAM Address 49)," on page 90 updated.
- "PSUM: Total Calculated Power (RAM Address 50)," on page 90 updated.
- "PTH12: Q1/Q2 Power Alarm Threshold (RAM Address 37)," on page 90 updated.
- "RINGOF: Ringing Waveform DC Offset (RAM Address 56)," on page 93 updated.
- "LCROFFHK: Loop Closure Detection Threshold—On-Hook to Off-Hook Transition (RAM Address 22)," on page 82 updated.
- "LCRONHK: Loop Closure Detection Threshold—Off-Hook to On-Hook Transition (RAM Address 23)," on page 82 updated.
- "SPEEDUPR: DC Settling Speedup Timer after Ringing (RAM Address 169)," on page 99 added.

Revision 0.95 to Revision 0.96

- Updated "Internal 16-Bit RAM Summary[1]," on page 57.

Revision 0.96 to Revision 0.97

- Updated "8-Bit Control Register Summary[1,2]," on page 7.
- Updated "Internal 16-Bit RAM Summary[1]," on page 57.
- Updated "Dual ProSLIC Initialization," on page 2.
- Updated Table 1, “RAM Values for 600 Ω. Impedance, Test Filters and Test Signal,” on page 3.
- Updated Register , “MSTRSTAT: Master Initialization Status (Register Address 3),” on page 27.
- Updated Register , “BATHTH: High Battery Switch Threshold (RAM Address 31),” on page 63.
- Updated Register , “BATLTH: Low Battery Switch Threshold (RAM Address 32),” on page 63
- Deleted Register “MSTREN: Master Initialization Enable (Register Address 2)”.
- Updated Register , “TXMODPWR: Transmit Path Modem Tone Power (RAM Address 124),” on page 115.

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