DUAL PROSLIC® LINE CARD DESIGN

Overview

The purpose of this application note is to facilitate line card design utilizing the Silicon Laboratories Si3220/Si3225 product family. The Si3220 can be used with the Si3200 integrated high-voltage linefeed device or, to achieve higher ringing voltages, with a discrete bipolar transistor linefeed. This application note is dedicated to the design of Si3220/Si3225 systems using the Si3200 integrated high-voltage linefeed device. This document relies extensively upon existing product data sheets, programming guides, and application notes. An overview of all available Si3220/Si3225 documentation, evaluation hardware, and software is provided.

The parametric design constraints and features that are applicable to a line card design are enumerated. Equations for determining chip set maximum permissible power dissipation, supply current requirements, and chip set power dissipation under various operating conditions are provided.

Thermal management, dc loop characteristics, ringing and ring trip characteristics (referencing “AN86: Ringing/ringtrip Operation And Architecture On The Si3220/Si3225”), PCB design characteristics (referencing “AN55: Si3220/Si3225 User Guide”), audio performance, surge protection, impedance synthesis, hybrid balancing and equalizer coefficient computation, and two- and four-wire return loss are each discussed with references to the applicable support documentation and software.

A Microsoft® Excel workbook is provided along with this application note to facilitate power consumption and power dissipation analysis. A design example is provided to illustrate the design process.

Contact your local Silicon Laboratories sales office or representative to obtain copies of the documents referenced herein and/or to obtain the various evaluation hardware kits and software.

Si3220/Si3225 Documentation

Table 1 provides a listing of the existing Si3220/Si3225 chipset documentation. When applicable, these documents are referenced for additional design information and additional detail.

Table 1. Si3220/Si3225 Documentation List

Ref. No.	Document Title
—	Si3220/Si3225 data sheet
AN39	Connecting the ProSLIC to the W&G PCM-4
AN55	Si3220/Si3225 User Guide
AN58	Si3220/Si3225 Programmer’s Guide
AN71	GR-909 Loop Testing Using the Si322x ProSLIC
AN86	Ringing/Ringtrip Operation and Architecture on the Si3220/Si3225
AN91	Si3200 Power Offload Circuit

Evaluation Hardware

Table 2 provides a list of evaluation hardware kits that are available for the Si3220/Si3225 product family. Table 3 provides a list of individual cards that are used in the hardware kits. Note that the individual cards enumerated in Table 3 are included in one or more of the kits shown in Table 2.

Table 2. Evaluation Hardware Kits

Order No.	Hardware Kit Description
Si3220PPT0-EVB	1 ProSLIC Motherboard 1 Si3220DC0-EVB Dual ProSLIC Daughter card Requires +5 V or +3.3 V bench power supply Requires two bench battery supplies (e.g. VBATL: –24 V and VBATH: –52 V or –78 V) May be used with SiLink-PS-EVB power supply card to supply +3.3 V/+5 V, VBATH and VBATL Requires host PC with LPT1 printer port for control Requires LINC Software
Si3225PPT0-EVB	1 ProSLIC Motherboard 1 Si3225DC0-EVB Dual ProSLIC Daughter card Requires +5 V or +3.3 V bench power supply Requires two bench battery supplies (e.g. VBATL: –26 V and VBATH: –56 V or –72 V) May be used with SiLinkPS-EVB power supply card to supply +3.3 V/+5 V, VBATH and VBATL Requires host PC with LPT1 printer port for control Requires LINC Software Requires external ring source
Si3220KIT4-EVB	2 Si3220DC0-EVB Daughter Cards 1 SiLink-PS-EVB Power Supply 1 SiLink uP-EVB 8-bit Microcontroller Card 1 120 VAC / 12 VDC Adapter - Standalone 4-channel PBX demo
Si3225KIT4-EVB	2 Si3225DC0-EVB Daughter Cards 1 SiLink-PS-EVB Power Supply 1 SiLink uP-EVB 8-bit Microcontroller Card 1 120 VAC / 12 VDC Adapter Four-channel PBX demo Requires external ring source

Table 3. Individual Evaluation Hardware Cards

Order No.	Hardware Card Description
Si3220DC0-EVB	Si3220 Dual ProSLIC Daughter card
Si3225DC0-EVB	Si3225 Dual ProSLIC Daughter card
SiLinkPS-EVB	1 Power Supply Card: V_{DD}: +5 V / +3.3 V (selectable) VBATL: –26 V VBATH: –52 V or –78 V (selectable) VBRNG: –96 V 1 12 VDC Adapter
SiLink-uP-EVB	8-bit Microcontroller Card

Table 4. Evaluation Hardware Documentation

Ref. No.	Document Title
AN68	8-bit Microcontroller Board Hardware Reference Guide
AN73	Si3220/Si3225 System Demonstration Kit User's Guide (for Si3320KIT4-EVB and Si3225KIT4-EVB)
AN74	SiLinkPS-EVB User's Guide
Si3220PPT-EVB	Si3220PPT0-EVB Documentation
Si3225PPT-EVB	Si3225PPT0-EVB Documentation

Evaluation Software

Table 5 provides a list of the existing Si3220/Si3225 evaluation software while Table 6 provides a list of the documents that support the evaluation software.

Table 5. Evaluation Software

Ref. No.	Software Title
—	Si3220/Si3225 LINC Software
—	Si3220/Si3225 Coefficient Generator
—	PC PBX and GR-909 Demo Software (C source code)
—	µP PBX and GR-909 Demo Software (C source code)

Table 6. Evaluation Software Documentation

Ref. No.	Document Title
AN63	Si322x Coefficient Generator User's Guide
AN64	Dual ProSLIC LINC User Guide
AN73	Si3220/Si3225 System Demonstration Kit User's Guide (for Si3320KIT4-EVB and Si3225KIT4-EVB µP kits and µP-DEMO-SW)
AN75	Si322x Dual ProSLIC Demo PBX and GR-909 Loop Testing Software Guide (PC-DEMO-SW)

Design Process

This section provides the information necessary to make the selection between the Si3220 and Si3325 and the appropriate device temperature grade. Design equations are provided to compute maximum chip set power dissipation and V_{DD} and V_{BAT} supply current requirements under all operating states.

Si3220 vs. Si3225 Selection

The key difference between the Si3220 and Si3225 is the ringing method.

The Si3220 offers internal balanced/unbalanced ringing eliminating the need for a centralized bulk ringer and associated relays. Using the Si3200 integrated high-voltage linefeed device, the Si3220 can generate ringing up to a maximum of 65 Vrms. This level of ring is adequate for most short loop applications such as PBX and VoIP line cards.

Using a discrete bipolar linefeed, the Si3220 can generate ringing signals up to 113 Vrms.

The Si3225 uses external ringing (centralized bulk ringer) and can therefore drive longer loops using a centralized bulk ring generator and associated relays while using the Si3200 integrated high-voltage linefeed device. Thus, the Si3225 is suitable for long loop applications, such as DLC (Digital Loop Carrier) systems.

Design Constraints

An appropriate first step in designing a line card is to identify the key applicable parametric design constraints and product features that are to be supported by the design. Table 7 enumerates the relevant parametric design constrains.

The last section of this document provides a design example. In the design example, Table 7 is completed with the typical parameters applicable to a short loop VoIP application.

Table 7. Line Card Parametric Constraints

Parametric Constraints	Symbol	Min.	Typ.	Max.	Units
Maximum ambient temperature	$T_{a.max}$				^oC
Maximum loop length	$L_{w.max}$				Feet or Meters
Nominal wire resistance per unit length	r_w				Ω/ft or Ω/m
Min/Max CPE off-hook dc resistance	$R_{cpe.min}$ $R_{cpe.max}$				Ω
Nominal loop current requirements	I_{LIM}				mA
Audio signal overhead current	I_{BIAS}				mA
Maximum REN load or Minimum ring impedance magnitude	maxREN $\|Z_{REN.min}\|$				Unitless Ω
Minimum CPE ring voltage	$V_{ring.RMS.min}$				Volts
Nominal ring frequency	f_{ring}				Hz
Nominal supply voltage	V_{DD}				Volts
Nominal common-mode voltage	V_{CM}				Volts
Nominal overhead voltage	V_{OV}				Volts

Relevant Product Specifications

Table 8 provides those chip set specifications, which are relevant to the computations presented in this application note. For complete product specifications, refer to the Si3220/Si3225 data sheet.

Table 8. Si3220/Si3225 Relevant Specifications

Parametric Constraints	Symbol (Conditions)	Min.	Typ.	Max.	Units
Si3200 thermal resistance	θ_{ja}		55		$^oC/W$
Si322x thermal resistance	θ_{ja}		25		$^oC/W$
Si3200 maximum operating junction temperature	$T_{j.max}$		140		^oC
Si322x maximum operating junction temperature	$T_{j.max}$		140		^oC
Si3200 overhead V_{DD} supply current (applicable to all linefeed states)	$I_{DD.OH}$		110		µA
Si322x overhead supply current (Fwd/Rev **A**ctive state)	$I_{DD.OH.A}$ (V_{DD} = 5 V) $I_{DD.OH.A}$ (V_{DD} = 3.3 V)		38 22		mA mA
Si322x overhead supply current (V_{DD} = +5 V, **R**inging state)	$I_{DD.OH.R}$ (V_{DD} = 5 V) $I_{DD.OH.R}$ (V_{DD} = 3.3 V)		26 22		mA

Table 8. Si3220/Si3225 Relevant Specifications (Continued)

VBAT overhead current (Fwd/Rev **A**ctive state)	$I_{VBAT.OH.A}$ (ABIAS = 4 mA)		4.4		mA
Nominal ring source impedance	R_{OUT}		320		W

Product Features and Regulatory Requirements

Table 9 enumerates the design features and regulatory requirements that may apply to the product.

Table 9. Product Definition and Features

Feature List	Applicable Specification(s)
Application	DLC/PBX/VoIP/IVD
Protection environment (over-voltage/over-current)	Bellcore GR-1089 ITU-T K.20, K.21 UL497A UL60950/EN60950
2-wire impedances (2-wire return loss)	Country List
Signaling requirements (pulse dialing, DTMF dialing)	Country List
Internal/External ring generation	Short/Long Loop
Preferred digital interface (Control and PCM data)	SPI + PCM Or GCI
Companding method	μ-Law / A-Law
Testing requirements (Line and SLIC)	GR-909
Number of channels per card	Application Dependent

Temperature Grade Selection

The Si3220/Si3225 and Si3200 chipset is available in two temperature grades (see Table 2 in DS-Si322x). The designer must select the temperature grade that satisfies the desired operating temperature range of the system.

See the Dual ProSLIC Product Selection Guide on page 2 of DS-Si322x for part ordering information.

Maximum Permissible Power Dissipation

The maximum power dissipation for the Si3200 or Si3220/Si3225 devices is obtained from Equation 1. The maximum junction temperature ($T_{j.max}$) and junction-to-ambient thermal resistance (θ_{ja}) are specified in the Si3220/Si3225 data sheet. For convenience, these parameters are reproduced in Table 10. The system designer supplies the maximum expected ambient temperature ($T_{a.max}$). The system designer must ensure that $P_{d.max}$ will not be exceeded for either device under the worst-case operating conditions.

$$P_{d.max} = \frac{T_{j.max} - T_{a.max}}{\theta_{ja}}$$

Equation 1.Maximum Power Dissipation

Table 10. Si3200 and Si3220/Si3225 Thermal Parameters

Device	Parameter	Value	Units
Si3200	θ_{ja}	55	^{o}C/Watt
	$T_{j.max}$	140	^{o}C
Si3220/Si3225	θ_{ja}	25	^{o}C/Watt
	$T_{j.max}$	140	^{o}C

In order to achieve the θ_{ja} values shown in Table 10, the PCB design must provide a suitably-designed heat slug. A heat slug is a heat-dissipating copper fill PCB structure under each device. See "PCB Design Guidelines" in this document for information concerning proper heat slug design for the Si3200 and Si3220/Si3225.

Ringer Impedance

This application note makes use of the North American Ringer Equivalence Number (REN) for defining ringer impedance (Telecordia GR-57). Equation 2 defines ringer impedance as a function of REN and ringing frequency, and Equation 3 provides the ringer impedance magnitude as a function of REN and ringing frequency. Equation 4 provides a simplified way to calculate the magnitude of the ringer impedance as a function of REN assuming a 20 Hz ring frequency. For simplicity, the definition in Equation 4 will be used throughout this document to compute ringer impedances.

$$Z_{ring}(REN, f_{ring}) = \frac{R}{REN} + \frac{1}{j \times 2 \times \pi \times f_{ring} \times C \times REN}$$

where,

$R = 6930\ \Omega$

$C = 8\ \mu F$

f_{ring} = ring_frequency

Equation 2.Ringer Impedance as a Function of REN and f_{ring}

$$\left|Z_{ring}(REN, f_{ring})\right| = \sqrt{\left(\frac{6930\Omega}{REN}\right)^2 + \left(\frac{1}{2 \times \pi \times f_{ring} \times 8 \times 10^{-6}F \times REN}\right)^2}$$

Equation 3.Magnitude of Ringer Impedance as a Function of REN and f_{ring}

$$\left|Z_{ring}(REN, 20\ Hz)\right| = \frac{7000\ \Omega}{REN}$$

Equation 4.Simplified Ringer Impedance Magnitude as a Function of REN (f_{ring} = 20 Hz)

Battery Voltages and Ringing Voltage Selection

In most applications, the Si3220/Si3225 will be used in conjunction with two battery supplies (termed VBATH and VBATL). The use of two battery supplies helps minimize chip set power dissipation while off-hook into shorter loops. SLIC battery voltages are always negative voltages.

The following paragraphs develop the requirements needed to determine the permissible range for VBATL and VBATH.

VBATL Selection (Si3220 and Si3225)

Equation 5 yields the voltage value of VBATL that is required to provide a CPE with maximum dc resistance with I_{LIM} (programmable from 18 mA to 45 mA) over a zero length loop while satisfying V_{CM} and V_{OV}. Note that $VBATL_{MIN}$ is not a practical battery voltage to use, since it would only support a loop of zero length, requiring switching to VBATH at extremely short loop lengths. However, $VBATL_{MIN}$ is useful in establishing a suitable range of voltage values for VBATL. Thus, $VBATL_{MIN}$ can be used together with $VBATL_{MAX}$ to select a VBATL value that is in the midway between the two.

$$\left|VBATL_{MIN}\right| = I_{LIM} \times R_{cpe.max} + V_{CM} + V_{OV}$$

Equation 5.Minimum VBATL

In the Fwd/Rev Active Off-Hook state, while operating on short loops and, therefore, while using VBATL, the worst-case power dissipation in the Si3200 occurs when the loop length is zero and the CPE exhibits the minimum expected off-hook dc resistance (Equation 6).

$$P_{Si3200} = (I_{LIM} + I_{BIAS}) \times \left|V_{BAT}\right| - R_{cpe.min} \times I_{LIM}^{2}$$

Equation 6.Power Dissipated in the Si3200 (at zero loop length)

Equation 7 is derived from Equation 6 and gives the maximum acceptable value for VBATL. The maximum voltage value for VBATL given by Equation 7 is such that the Si3200 power dissipation does not exceed $P_{d.max}$, as determined by Equation 1 for the Si3200 when the loop length is zero. Equation 7 provides a means of computing the maximum VBATL using a margin factor, k. For example, let k = 0.90 so that the maximum power dissipation at zero loop length will be 90% of $P_{d.max}$ (10% safety margin).

$$|VBATL_{MAX}| = \frac{k \times P_{d(max)} + R_{cpe.min} \times I_{LIM}^2}{I_{LIM} + I_{BIAS}}$$

Equation 7.Maximum VBATL

The selected |VBATL| voltage must be between $|VBATL_{MIN}|$ and $|VBATL_{MAX}|$. The larger the selected value of |VBATL| (without exceeding $|VBATL_{MAX}|$), the longer the loop that can be serviced by VBATL from a dc feed standpoint. Also, choosing a larger value for VBATL will reduce the worst-case power dissipation when it becomes necessary to switch to VBATH. The worst-case power dissipation when operating with VBATL and VBATH is best illustrated by the Excel workbook that complements this application note (see "Excel Design Tool," on page 17).

VBATH Selection (Si3220)

During internal ringing generation, the Si3220 will automatically use VBATH as the battery supply. CPE ringers will properly respond to a ringing signal (produce an audible ring sound) if the RMS value of the ringing signal arriving at the CPE meets a certain minimum value ($V_{ring.CPE.rms}$). Therefore, the ringing signal sourced at the SLIC must take into consideration the dc resistance of the longest possible loop and the maximum REN load at the CPE. Equation 8 is obtained by a simple voltage division derivation. Note that internal ringing generation in the Si3220 is limited to a maximum of 65 Vrms when using the Si3200 linefeed device. This limit on the ringing signal amplitude is imposed by the maximum voltage rating of the Si3200 linefeed, which is 100 V. It is possible to achieve higher internal ringing levels with the Si3220 by using a discrete bipolar transistor linefeed with transistors rated for 160 V or more.

$$V_{ring.RMS.min} = \frac{R_{OUT} + R_{loop.max} + |Z_{ring}(maxREN)|}{|Z_{ring}(maxREN)|} \times V_{ring.CPE.min}$$

where

$V_{ring.RMS.min} \leq 65\ V_{rms}(Si3200)$

$V_{ring.RMS.min} \leq 113\ V_{rms}(discrete\_BJT\_linefeed)$

Equation 8.Minimum Required Ring Level ($V_{ring.RMS.min}$)

where

- R_{OUT} is the output impedance of the Si3220 during internal ringing generation in Ohms
- $R_{loop.max}$ is the maximum dc resistance of the loop in Ohms (longest loop)
- $|Z_{ring}(maxREN)|$ is the magnitude of the CPE ringer at maximum REN in Ohms (e.g. 7000 Ω/maxREN).
- $V_{ring.CPE.min}$ is the minimum required ringing voltage delivered to the CPE in volts RMS
- $V_{ring.RMS.min}$ is the minimum required ringing voltage at the Si3220 source in volts RMS

The excursion of an internally-generated balanced/ unbalanced ring signal in the Si3220 is confined between the GND and VBATH rails. Therefore, the VBATH battery voltage must be able to sustain the peak voltage associated with the minimum ringing signal as determined by Equation 8 plus the ringing dc offset (V_{OFF}), if any, as shown in Equation 9.

See “AN86: Ringing/Ringtrip Operation and Architecture of the Si3220/Si3225” for information on determining whether a ring dc offset is required and how to determine its optimal value.

$$|VBATH_{MIN}| = V_{ring.RMS.min} \times \sqrt{2} + V_{OFF}$$

where

$V_{ring.RMS.min}$ is the minimum required RMS ringing voltage at the source (sinusoidal)

and

V_{OFF} is the dc offset of the ringing voltage

Equation 9.Minimum VBATH (Sinusoidal Ring)

For dc feed purposes, the Si3220 will automatically switch to VBATH when it detects that VBATL is insufficient to satisfy the overhead voltage requirement (V_{CM} + V_{OV}). See "Battery Switching Threshold," on page 9 for information on how to program the battery switching thresholds in the Si3220. While using VBATH, the maximum power dissipation in the Si3200 linefeed device occurs in the off-hook state at the minimum loop length that requires VBATH in order to satisfy the overhead voltage requirements (V_{CM} + V_{OV}). Equation 10 gives the dc resistance of the loop plus CPE at which

battery switching from VBATL to VBATH will occur since VBATL can no longer sustain the required overhead voltages.

$$R_{SW} = \frac{|V_{BATL}| - V_{CM} - V_{OV}}{I_{LIM}}$$

Equation 10.Total Loop Resistance at Battery Switching Point

Equation 11 gives |VBATHmax|, such that the power dissipation in the Si3200 will not exceed $P_{d.max.Si3200}$. The factor, k, provides margin. For example, choose k = 0.9 so that the maximum power dissipation in the Si3200 will be 90% of $P_{d.max.Si3200}$ while using VBATH.

$$|VBATH_{MAX}| = \frac{k \times P_{d.max.Si3200} + (|V_{BATL}| - V_{CM} - V_{OV}) \times I_{LIM}}{I_{LIM} + I_{BIAS}}$$

Equation 11.Maximum VBATH

The selected |VBATH| voltage must be between $|VBATH_{min}|$ and $|VBATH_{max}|$.

VBATH Selection (Si3225)

The Si3225 uses an external bulk ringer and controls the associated relays. Therefore, the external bulk ringer must be able to supply the necessary ringing voltage as expressed by Equation 8. Since ringing is being generated externally, it does not play a role in determining VBATH. Instead, the VBATH range for the Si3225 is governed by the minimum voltage requirements to feed dc to the loop while meeting the overhead voltage requirements (V_{CM} and V_{OV}) and by the maximum power dissipation considerations for the Si3200 linefeed device.

For the maximum loop length and while operating in the Fwd/Rev Active off-hook state, VBATH must be able to supply enough voltage to the loop (V_{TR}), and maintain the required overhead voltages (V_{CM} + V_{OV}). This requirement is expressed in Equation 12.

$$|VBATH| \geq V_{TR} + V_{CM} + V_{OV}$$

Equation 12.DC Feed Battery Voltage Requirement

V_{TR} is simply the product of I_{LIM} and the total dc resistance of the loop as shown in Equation 13.

$$V_{TR} = I_{LIM} \times (r_w \times L_w \times R_{cpe})$$

Equation 13.TIP-RING Voltage

Equation 14 is readily formed from Equation 12 and Equation 13 for a loop of maximum length and with a CPE of maximum off-hook dc resistance. The proper selection of the battery switching threshold, as detailed in "Battery Switching Threshold," on page 9, guarantees that VBATL will sustain the required overhead voltages (V_{CM} + V_{OV}) up to the point where the Si3225 will automatically switch to VBATH. Meanwhile, VBATH should satisfy Equation 14 up to the longest loop length expected by the application. However, in cases where the total maximum loop resistance is too large to achieve I_{LIM} and meet V_{CM} and V_{OV}, the linefeed will operate in the constant voltage region with a loop current that is less than I_{LIM}.

The requirement given in Equation 14 applies to both the Si3220 and Si3225 to ensure that the overhead voltages will be met at the longest possible loop length.

$$|VBATH_{MIN}| = I_{LIM} \times (r_w \times L_{w.max} + R_{cpe.max}) + V_{CM} + V_{OV}$$

Equation 14.Battery Overhead Requirement

VBATH must also be sufficient to supply V_{OC} + V_{CM} + V_{OV} in the on-hook Fwd/Rev active standby state, as shown in Equation 15, where V_{OC} is the programmed open-circuit (i.e. I_{LOOP} = 0) $V_{TIP} - V_{RING}$ voltage.

$$|VBATH_{MIN}| \geq V_{OC} + V_{CM} + V_{OV}$$

Equation 15.VBATH On-Hook Requirement

Equation 14 can be re-written to calculate the theoretical maximum loop length supported by V_{BAT} from a dc feed viewpoint, as shown in Equation 16.

$$L_{w.max} = \frac{1}{r_w} \times \left(\frac{|V_{BAT}| - V_{CM} - V_{OV}}{I_{LIM}} - R_{cpe.max} \right)$$

Equation 16.Maximum Loop Length Supported by V_{BAT}

The $|VBATH_{max}|$ voltage for the Si3225 is determined by Equation 17, based on maximum permissible power dissipation and margin factor k.

$$|VBATH_{MAX}| = \frac{k \times P_{d.max.Si3200} + (|V_{BATL}| - V_{CM} - V_{OV}) \times I_{LIM}}{I_{LIM} + I_{BIAS}}$$

Equation 17.Maximum VBATH

The selected |VBATH| voltage must be between $|VBATH_{min}|$ and $|VBATH_{max}|$.

Single Battery Applications

Some applications may have a single negative battery supply voltage available in the system. See "AN95: Si3200 Power Offload Circuit" for detailed information on the design of a suitable power offload circuit for the Si3200, which can be used to minimize power dissipation on short loops in cases where a single battery supply is available in the system.

Battery Switching Threshold

The Si322x battery switching mechanism monitors the dc voltage at the RING terminal (TIP in reverse active mode). The RING voltage with respect to system GND already includes V_{CM}; therefore, the switching threshold is obtained from Equation 18.

$$V_{thres} = |V_{BATL}| - V_{OV}$$

Equation 18.Battery Switching Threshold Voltage

The RAM locations, BATHTH and BATLTH, can be programmed with a value in the range from 0 to 160.8 in volts. One LSB of BATHTH or BATLTH is 628 mV. The values for BATHTH and BATLTH occupy bits 7 through 14 in their corresponding register and must be shifted up by 7 bit positions, hence the multiplication by 2^7 in Equation 19 and Equation 11.

Equation 19 and Equation 11 provide a means of calculating BATHTH and BATLTH, which provides for 2 LSBs of hysteresis (2 x 0.628 = 1.256V). Greater amounts of hysteresis are possible by modifying Equation 19 and Equation 11.

$$BATHTH = 2^7 \times DEC2HEX\left(\left(\frac{V_{thres}}{0.628}\right) + 1\right)$$

Equation 19.Equation for BATHTH

$$BATLTH = 2^7 \times DEC2HEX\left(\left(\frac{V_{thres}}{0.628}\right) - 1\right)$$

Equation 20.

The value of BATLPF is obtained from Equation 21, where f is the desired cut-off frequency for the low-pass filter. BATLPF occupies bits 3 through 15 in its corresponding RAM location and must be shifted up three bit positions, hence the multiplication by 2^3 in Equation 21. Typically, f is set to 10 Hz, which yields BATLPF = 0xA10.

$$BATLPF = 2^3 \times DEC2HEX\left(\frac{2 \times \pi \times f \times 4096}{800}\right)$$

Equation 21.Equation for BATLPF

Refer to "AN58: Si3220/Si3225 Programmer's Guide" for all register and RAM location definitions.

Sleep, Open, On-Hook Active Standby and OHT States

The supply current and power dissipation applicable to the Sleep, Open, On-Hook Active Standby and On-Hook Transmit states are provided in Table 3 (for V_{DD} = +3.3 V) and Table 4 (for V_{DD} = +5 V) in the Si3220/Si3225 data sheet. The specified currents and power dissipations given in these tables are per-channel. These specifications are reproduced in Tables 11 and 12 for convenience.

Table 11. I_{DD} for Sleep, Open, Standby, and OHT States

Symbol	Conditions	V_{DD} = +3.3 V	V_{DD} = +5 V	Units
$I_{DD.SLEEP}$	RESET/ = 0	1	1	mA
$I_{DD.OPEN}$		15	20	mA
$I_{DD.STBY}$		15	20	mA
$I_{DD.OHT}$	OBIAS = 4 mA	44	60	mA

Table 12. I_{VBAT} for Sleep, Open, Standby and OHT States

Symbol	Conditions	V_{DD} = +3.3 V	V_{DD} = +5 V	Units
$I_{VBAT.SLEEP}$	VBAT = –70 V	100	100	μA
$I_{VBAT.OPEN}$	VBAT = –70 V	225	225	μA

Table 12. I_{VBAT} for Sleep, Open, Standby and OHT States (Continued)

$I_{VBAT.STBY}$	VBAT = –70 V	400	400	µA
$I_{VBAT.OHT}$	VBAT = –70 V OBIAS = 4 mA	8.4	8.4	mA

The currents and power dissipations associated with the Sleep, Open, On-Hook Active Standby, and OHT states are well under the worst-case values and, therefore, do not set the requirements for power supply currents and overall chip set power dissipation.

- The Sleep state occurs while the RESET pin is held low.
- The Open state refers to LINEFEED = 0.
- The On-Hook Active (Fwd/Rev) standby state refers LINEFEED = 1 or 5 while the CPE is in the on-hook state (i.e. I_{LOOP} = 0).
- The OHT (Fwd/Rev) state refers to LINEFEED = 2 or 6.

The worst-case supply current requirements and device power dissipations occur either in the Off-Hook Fwd/Rev Active state (LINEFEED = 1, off-hook) or in the ringing state, which are covered in later sections.

Refer to “AN58: Si3220/Si3225 Programmer’s Guide” for all register and RAM location definitions.

Supply Current (Fwd/Rev Active Off-Hook)

The supply currents required from V_{DD} and V_{BAT} in the Forward/Reverse Active Off-Hook state are provided in DS-Si322x in Table 3 (for V_{DD} = +3.3 V) and in Table 4 (for V_{DD} = +5 V). These specifications are reproduced in Equation 22 and Equation 23. The stated overhead currents assume an ABIAS setting of 4 mA. If ABIAS is increased, $I_{DD.OH.A}$ increases accordingly. Typically, an ABIAS setting of 4 mA is adequate for the vast majority of applications. I_{LIM} is the loop current limit programmed via the I_{LIM} register. The V_{DD} overhead supply current required by the Si3200 linefeed device ($I_{DD.OH}$) during the off-hook state is 110 µA (for ABIAS = 4 mA).

$$I_{DD.A} = I_{DD.OH.A} + I_{DD.OH} + I_{LIM}$$

Equation 22.I_{DD} (Fwd/Rev Active Off-Hook)

Equation 23 gives the current required from V_{BAT} during the forward/reverse off-hook active state.

$$I_{VBAT.A} = I_{VBAT.OH.A} + I_{LIM}$$

Equation 23.IVBAT (Fwd/Rev Active Off-Hook)

Power Dissipation (Fwd/Rev Active Off-Hook)

Equation 24 gives the power dissipated in the Si3200 linefeed device while sourcing dc power to the line and off-hook CPE.

$$P_{Si3200.A} = 1.02 \times (I_{LIM} + I_{BIAS}) \times (|V_{BAT}| + 0.7V) - (r_w \times L_w + R_{cpe}) \times I_{LIM}^2$$

Equation 24.Power Dissipated in the Si3200 Line Feed

where:

- $P_{Si3200.A}$ is the power dissipated in the Si3200 in watts.
- I_{LIM} is the off-hook loop current limit as set by the ILIM register in amperes.
- I_{BIAS} is the audio overhead current set by the ABIAS field in the SBIAS register in amperes.
- V_{BAT} is the battery voltage (may be set to VBATH or VBATL, depending on loop length).
- r_w is the resistance per unit length of the loop in ohms per unit length (feet or meters).
- L_w is the loop length in feet or meters.
- R_{cpe} is the off-hook dc resistance of the CPE in ohms.

While operating the dc feed with V_{BATL}, the worst-case power dissipation occurs at zero loop length and can be computed by letting $V_{BAT} = V_{BATL}$ and $L_w = 0$ in Equation 24, resulting in Equation 25.

$$P_{Si3200.A} = 1.02 \times (I_{LIM} + I_{BIAS}) \times (|V_{BAT}| + 0.7V) - R_{cpe.min} \times I^2_{LIM}$$

Equation 25.$P_{Si3200.A}$ (worst-case @ VBATL)

While operating the dc feed with VBATH, the worst-case power dissipation occurs at the loop length that results in the battery switching from VBATL to VBATH and can be obtained by letting VBAT = VBATH and r_w x L_w + $R_{cpe.min}$ = R_{SW} in Equation 24. R_{SW} is given by Equation 10.

$$P_{Si3200.A} = 1.02 \times (I_{LIM} + I_{BIAS}) \times (|V_{BATH}| + 0.7V) - (|V_{BATL}| - V_{CM} - V_{OV}) \times I_{LIM}$$

Equation 26.$P_{Si3200.A}$ (worst-case @ VBATH)

Equation 27 is used to calculate the power dissipated in the Si3220/Si3225 during the Forward/Active Off-Hook state.

$$P_{Si322x.A} = (V_{DD} - 0.7V) \times I_{LIM} + V_{DD} \times I_{DD.OH.A}$$

Equation 27.Power Dissipated in the Si322x

where:

- $P_{Si322x.A}$ is the power dissipated in the Si3220/ Si3225 in watts
- V_{DD} is the power supply rail (+5 V or +3.3 V)
- I_{LIM} is the loop current as set by the ILIM register in amps
- $I_{DD.OH.A}$ is the Si322x V_{DD} overhead current (38 mA @ V_{DD} = +5 V or 22 mA @ V_{DD} = +3.3 V)

Equation 24 through Equation 27 assume that the dc feed will enter into the constant current region, such that the loop current will equal I_{LIM}. If the loop dc resistance is such that I_{LIM} cannot be reached, the dc feed will operate in the constant voltage region with a loop current less than I_{LIM}, and the power dissipation will be reduced accordingly. See "DC Feed Characteristics," on page 13.

Supply Current (Internal Sinusoidal Ringing)

The push-pull linefeed architecture of the Si3220 and Si3200 chipset results in a full-wave rectified supply current demand during sinusoidal ringing generation.

Equation 28 gives the average value of a full-wave rectified sinusoid of peak amplitude A as $2/\pi$ x A.

$$\frac{1}{T} \times \int_0^T |A \times \sin(2 \times \pi \times f \times t)| \times dt = \frac{2}{\pi} \times A$$

where

$$T = \frac{1}{f}$$

Equation 28.Average Value of a Full-Wave Rectified Sinusoid

Equation 29 gives the average power supply current during sinusoidal ringing generation required from the V_{DD} and V_{BAT} rails per-channel to drive the loop. The loop impedance magnitude ($|Z_{loop}|$) is the sum of the dc resistance of the twisted pair wire (R_{loop}), the magnitude of the ringer impedance of the CPE ($|Z_{ring}(REN)|$) and the output impedance of the SLIC during ringing generation (R_{OUT}=320 Ω).

$$I_{AVE.RING.SINE} = \frac{V_{ring.pk}}{|Z_{loop}|} \times \frac{2}{\pi}$$

where

$$|Z_{loop}| = R_{loop} + |Z_{ring}(REN)| + R_{OUT}$$

Equation 29.Average Ringing Current

$V_{ring.pk}$ is the programmed ringing amplitude or open loop ringing voltage.

Equation 30 gives the current required from the V_{DD} rail during ring.

$$I_{DD.R} = I_{AVE.RING.SINE} + I_{DD.OH.R}$$

where

$$I_{DD.OH.R} = \begin{cases} 26 \text{ mA @ } V_{DD} = +5 \text{ V} \\ 22 \text{ mA @ } V_{DD} = +3.3 \text{ V} \end{cases}$$

Equation 30.Average IDD Ringing Supply Current (Sinusoidal Ring)

Equation 31 gives the current required from the V_{BAT} rail during ringing generation.

$$I_{VBAT.R} = I_{AVE.RING.SINE}$$

Equation 31.IVBAT Ring Supply Current (Sinusoidal Ring)

The V_{DD} rail and the V_{BAT} rail must each be capable of supplying their respective supply currents multiplied by the maximum number channels that may simultaneously generate a ringing signal.

Power Dissipation (Internal Sinusoidal Ringing)

The worst-case power dissipation in the Si3200 and Si3220 during internal ringing generation occurs when the loop length is zero and the ringer impedance of the CPE is at the minimum expected value (i.e. maximum REN). Ringer impedance magnitude as a function of REN is defined in Equation 3.

Equation 32 gives the power dissipated in the Si3200 linefeed device during sinusoidal ringing generation. The term $I_{AVE.RING.SINE}$ is defined in Equation 29.

$$P_{Si3200.R} = (|V_{BAT}| + 0.7V) \times I_{AVE.RING.SINE} + I_{DD.OH} \times (V_{DD} + |V_{BAT}|) - I^2_{LOOP.RMS.SINE} \times (|Z_{ring}(REN)| + R_{loop})$$

where

$$I_{LOOP.RMS.SINE} = \frac{V_{RMS.SINE}}{R_{LOOP} + |Z_{ring}(REN)|}$$

Equation 32.Si3200 Power Dissipation (Sinusoidal Ring)

Equation 33 gives the power dissipated in the Si3220 during sinusoidal internal ringing generation.

$$P_{Si3220.RING.SINE} = V_{DD} \times I_{DD.OH.R} + (V_{DD} - 0.7V) \times I_{AVE.RING.SINE}$$

where

$$I_{DD.OH.R} = \begin{cases} 26\text{ mA @ } V_{DD} = +5\text{ V} \\ 22\text{ mA @ } V_{DD} = +3.3\text{ V} \end{cases}$$

Equation 33.Si3220 Power Dissipation (Sinusoidal Ring)

Supply Current (Internal Trapezoidal Ringing)

The Si3220 can be programmed to generate a trapezoidal ringing signal. Provided that the added harmonic content is not objectionable, a trapezoidal ringing signal may be used instead of a sinusoidal ringing signal in cases where a greater crest-factor is desired. Crest-factor is defined as the ratio of the peak voltage and RMS voltage, as shown in Equation 34.

The push-pull linefeed architecture of the Si3220 and Si3200 chipset results in a full-wave rectified supply current demand during ringing generation. The rise time of the trapezoidal signal is computed from the desired crest factor (CF), as shown in Equation 35. The average value for a full-wave rectified trapezoidal waveform is as given in Equation 36.

$$CF = \frac{V_{pk}}{V_{rms}}$$

Equation 34.Crest Factor (CF)

$$t_{rise} = \frac{3}{4 \times f_{ring}} \times \left(1 - \frac{1}{CF^2}\right)$$

Equation 35.Rise Time as a Function of CF and Ringing Frequency

$$1 - \frac{t_{rise}}{T_{ring}}$$

Equation 36.Average Value of a Full-Wave Rectified Trapezoid

Equation 37 gives the average ringing current delivered to the loop during trapezoidal ringing.

$$I_{AVE.RING.TPZ} = \frac{V_{ring.pk}}{|Z_{loop}|} \times \left(1 - \frac{t_{rise}}{T_{ring}}\right)$$

where

$$Z_{loop} = R_{loop} + |Z_{ring}(REN)| + R_{OUT}$$

Equation 37.Average Ring Current (Trapezoidal)

Equation 38 gives the I_{DD} supply current required during trapezoidal ringing.

$$I_{DD.RING.TPZ} = I_{AVE.RING.TPZ} + I_{DD.OH.R}$$

where

$$I_{DD.OH.R} = \begin{cases} 26\text{ mA @ } V_{DD} = +5\text{ V} \\ 22\text{ mA @ } V_{DD} = +3.3\text{ V} \end{cases}$$

Equation 38.I_{DD} Supply Current (Trapezoidal Ring)

Equation 39 gives the I_{VBAT} supply current required during trapezoidal ringing.

$$I_{VBAT.RING.TPZ} = I_{AVE.RING.TPZ}$$

Equation 39.I_{VBAT} Supply Current (Trapezoidal Ring)

Power Dissipation (Internal Trapezoidal Ringing)

Equation 40 provides the power dissipated in the Si3200, and Equation 41 provides the power dissipated in the Si3220 during trapezoidal ringing; the term I_{AVE} is given by Equation 37.

$$P_{Si3200.RING.TPZ} = (|V_{BAT}| + 0.7V) \times I_{AVE.RING.TPZ} + I_{DD.OH} \times (V_{DD} + |V_{BAT}|) - I^2_{LOOP.RMS.TPZ} \times (|Z_{ring}(REN)| + R_{loop})$$

where

$$I_{LOOP.RMS.TPZ} = \frac{V_{RING.PK}}{CF}$$

Equation 40.Power Dissipated in the Si3200 (Trapezoidal Ringing)

$$P_{Si3220.RING.TPZ} = V_{DD} \times I_{DD.OH.R} + (V_{DD} - 0.7V) \times I_{AVE.RING.TPZ}$$

where

$$I_{DD.OH.R} = \begin{cases} 26\ mA\ @\ V_{DD} = +5\ V \\ 22\ mA\ @\ V_{DD} = +3.3\ V \end{cases}$$

Equation 41.Power Dissipated in the Si3220 (Trapezoidal Ring)

Thermal Management Considerations

Proper PCB design and air circulation are critical to proper line card design. The effective junction-to-ambient thermal resistance of a design is largely dependent on the design of PCB heat slug structures (copper fill) for the Si3200 and Si3220/Si3225 device packages.

Furthermore, the θ_{ja} of 55°C/W for the Si3200 and θ_{ja} of 25°C/W for the Si3220/Si3225 stated in Table 1 of the Si3220/Si3225 data sheet, assume a certain minimum PCB heat slug design (PCB copper fill under the chip packages). A proper solder bond between each device paddle and its corresponding PCB heat slug is also critical to achieving optimal θ_{ja}.

Refer to "AN55: Si3220/Si3225 User Guide" for detailed PCB design guidelines. Additionally, the system designer must carefully consider enclosure ventilation and proper airflow in order to guarantee the maximum ambient temperature that will be experienced by the line card design during worst-case operating conditions.

DC Feed Characteristics

The Si3220/Si3225 features a proprietary dc feed design known as adaptive linefeed.

Figure 1 shows the V/I characteristics of adaptive linefeed. Essentially, adaptive linefeed changes the source impedance of the dc feed as well as the open-circuit voltage (VOC) in order to ensure the ability to source extended loop lengths. The following sections provide a detailed explanation of adaptive linefeed. Also, see "DC Feed Characteristics" in the Si3220/Si3225 data sheet.

Adaptive Linefeed Example

This section provides a detailed description of adaptive linefeed operation by utilizing an example. The behavior of adaptive linefeed is controlled by the following RAM locations: VOV, VCM, VOC, VOCLTH, VOCHTH, and VOCDELTA (see Equation 42). The I_{LIM} register also plays a role in determining the behavior of the dc feed as it sets the current limit for the constant current source. I_{LIM} is a 5-bit register field, which is programmable from 18 mA to 45 mA in 0.875 mA steps (i.e. I_{LIM} = 0x0 corresponds to 18 mA and I_{LIM} = 0x1F corresponds to 45 mA).

$$RAMValue = DEC2HEX\left(2 \times CEILING\left(ROUND\left(\frac{desired\_voltage}{1.005\ V}\right) \times \frac{512}{5}\right)\right)$$

Equation 42.VOV, VCM, VOC, VOCLTH, VOCHTH, and VOCDELTA

In the above equation, the ROUND function rounds the result to the nearest integer while the CEILING function rounds-up the result to the nearest integer. The DEC2HEX function converts a decimal integer into a hexadecimal integer.

The RAM values shown in Table 13 where used to generate the adaptive linefeed V/I curve shown in Figure 1. Note that a battery voltage of –56 V was also assumed, as shown in Table 13. The value of VCM = 3 V provides sufficient voltage headroom to support a +3.1 dBm signal into a 600 Ω at an I_{LIM} setting of 22 mA. The value of VOV = 4 V provides sufficient headroom to support a +3.1 dBm signal into 600 W with an I_{LIM} setting of 45 mA. VOC is chosen as approximately VBAT – VCM – VOV, hence the value of –48 V.

Table 13. Adaptive Linefeed Example Values

VBAT	VOV	VCM	VOC	ILIM	VOCLTH	VOCHTH	VOCDELTA
–56 V	4 V	3 V	–48V	20 mA	–7 V	+2 V	+6 V

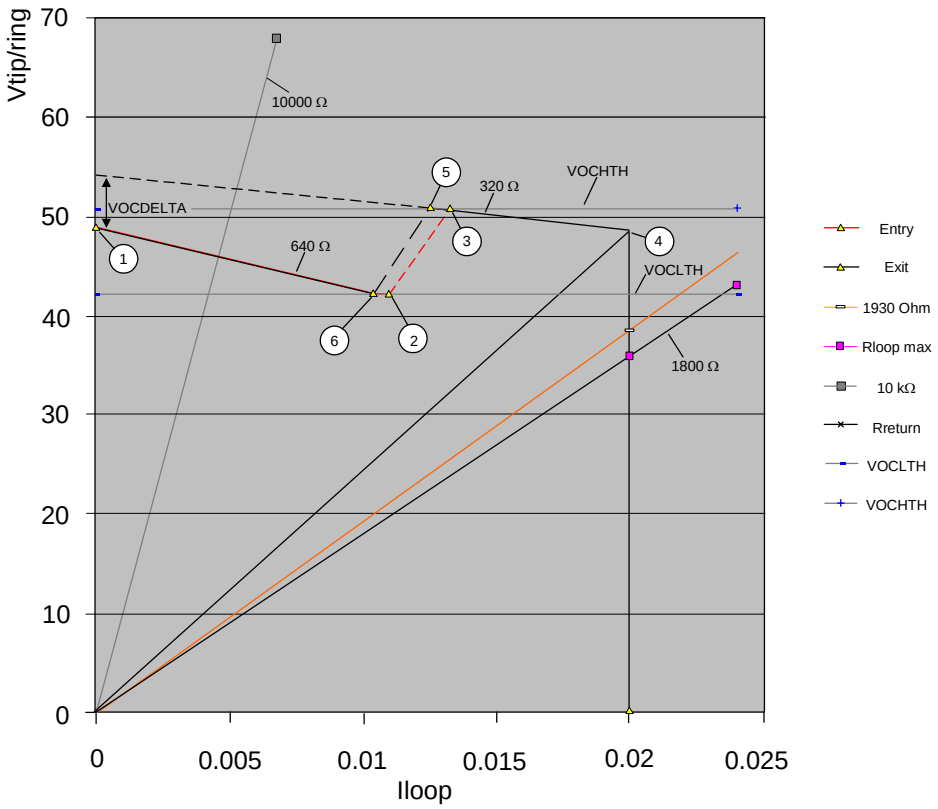

Figure 1. V/I Behavior

When the Si3220/Si3225 is used with the Si3200 linefeed device, the source impedance of the dc feed is 640 Ω before the adaptive linefeed transition and 320 Ω after the adaptive linefeed transition, as shown in Figure 1. Alternatively, when the Si3220/Si3225 is used with a discrete bipolar transistor linefeed, the source impedance of the dc feed is 320 Ω both before and after the adaptive linefeed transition.

On-Hook to Off-Hook Transition

Referring to Figure 1, point (1) represents the open-circuit voltage (VOC = –48 V) of the dc feed. At point (1), the source impedance of the dc feed is 640 Ω (320 Ω for discrete bipolar transistor linefeed) and V_{TR} = VOC, since no current flows in the loop. When a dc load is connected across TIP and RING, and as dc current begins to flow in the dc loop, the product of the dc loop current and the 640 Ω (320 Ω for a discrete bipolar transistor linefeed) source impedance causes the V_{TR} voltage to decline linearly with increasing loop current. When the V_{TR} voltage reaches the VOCLTH threshold (point 2), adaptive linefeed switches the source impedance of the dc feed to 320 Ω and simultaneously boosts the value of VOC by VOCDELTA (point 3). The source impedance of the dc feed will now remain at 320 Ω until the programmed current limit (I_{LIM}) is reached (point 4). At point (4), the dc feed has entered into the constant current mode of operation.

Off-Hook to On-Hook Transition

As the dc loop is opened, the dc feed will exit the constant current region (point 4) and enter the 320 Ω source impedance region. As the current in the loop collapses, the V_{TR} voltage will linearly increase until VOCHTH (point 5) is reached. At this point, adaptive linefeed will transition to a source impedance of 640 Ω (320 Ω for discrete bipolar transistor linefeed) and decrease the VOC voltage by VOCDELTA (point 6).

VOCTRACK and Adaptive Linefeed Hysteresis

The two thresholds, VOCLTH and VOCHTH, control adaptive linefeed hysteresis as seen in Figure 1. As described in the previous sections, VOCLTH is the V_{TR} voltage threshold at which adaptive linefeed will transition from a source impedance of 640 Ω (320 Ω for discrete bipolar transistor linefeed) to a source impedance of 320 Ω, while at the same time increasing VOC by VOCDELTA during the on-hook to off-hook transition. Conversely, VOCHTH is the threshold at which adaptive linefeed transitions from a source

impedance of 320 Ω to a source impedance of 640 Ω (320 Ω for discrete bipolar transistor linefeed), while at the same time decreasing VOC by VOCDELTA.

VOCTRACK is a RAM location and is the actual open-circuit voltage that is being fed to the line. VOCTRACK is dependent on the measured V_{BAT} voltage. The behavior of VOCTRACK is as shown in Equation 43. Simply put, as long as V_{BAT} is sufficient to supply VOC + VOV + VCM, VOCTRACK is equal to the programmed VOC. However, if V_{BAT} becomes too small to support VOC + VOV + VCM, VOCTRACK will track the battery voltage so that the programmed VOV and VCM are satisfied at the expense of a reduced VOC voltage. In the example of Figure 1,

$$|VBAT| = 56\ V \cong VOC + VOV + VCM$$

therefore

$$VOCTRACK = VOC = 48\ V$$

$$|V_{BAT}| \geq V_{OC} + V_{OV} + V_{CM} \Rightarrow VOCTRACK = VOC$$

$$|V_{BAT}| < V_{OC} + V_{OV} + V_{CM} \Rightarrow VOCTRACK = |V_{BAT}| - (V_{OV} + V_{CM})$$

Equation 43.VOCTRACK Behavior

The values of VOCLTH and VOCHTH are set relative to VOCTRACK. In the example of Figure 1, VOCLTH is given as –7 V and VOCHTH as +2 V. This implies that the VOCLTH threshold is located seven volts below the prevailing value of VOCTRACK while the VOCHTH threshold is located two volts above the prevailing value of VOCTRACK. Therefore, the VOCLTH and VOCHTH thresholds will automatically track the battery voltage along with VOCTRACK.

In order to provide an adequate level of adaptive linefeed hysteresis between the on-hook to off transition and the off-hook to on-hook transition, VOCLTH is programmed to be below VOCTRACK (e.g. –7 V relative to VOCTRACK) and VOCHTH is programmed above VOCTRACK (e.g. +2 V above VOCTRACK). Also, VOCHTH must be less than VOV – 1 V, to ensure that a proper adaptive linefeed transition will occur in a reduced battery scenario.

Dual ProSLIC® Coefficient Generation

Silicon Laboratories provides an Si3220/Si3225 Coefficient Generator Windows® application that is used to synthesize 2-wire impedance synthesis coefficients, 4-wire echo cancellation coefficients, and transmit and receive equalizer coefficients. The designer must supply the specifications for the desired 2-wire impedance (the impedance that the SLIC must present to the line), hybrid balancing impedance (the impedance presented by the line to the SLIC), and the desired transmit/receive frequency response.

The Si322x/Si3200 chipset provides programmable impedance synthesis architecture capable of satisfying 2-wire return loss requirements around the world. The designer must identify the list of 2-wire terminating impedances that are required for the application and generate coefficients for each one of the required impedances. Already synthesized coefficients for most countries around the world are also available from Silicon Laboratories.

The Coefficient Generator also synthesizes coefficients for balancing the echo cancellation path within the SLIC in order to provide a sufficiently large 4-wire return loss (far-end echo return loss). The impedance used to balance the echo cancellation path may be the same, or it may differ from the 2-wire return loss impedance synthesized by the SLIC.

Finally, the Coefficient Generator also synthesizes TX and RX equalizer coefficients to meet a user-specified transmit and receive gain versus frequency response.

Refer to:

- “AN63: Si322x Coefficient Generator User’s Guide”
- Si322x Coefficient Generator Windows® Application

Ringing and Ring Trip Characteristics

Ringing and ring trip characteristics of the Si3220 and Si3225 are covered in detail in “AN86: Ringing/Ringtrip Operation and Architecture on the Si3220/Si3225”.

Audio Performance

The audio performance specifications for the Si3220/Si3225 can be found in Table 5 of the Si3220/Si3225 data sheet.

Since audio performance may be detrimentally affected by the characteristics of the Printed Circuit Board (PCB) design, it is extremely important that proper PCB design guidelines be followed. Refer to “PCB Design Guidelines” in this document.

Furthermore, line card performance should be thoroughly verified against industry standard requirements using equipment, such as the Wandel & Goltermann PCM-4.

Refer to:

- Table 5 “AC Characteristics” in the Si3220/Si3225 data sheet
- “AN39: Connecting the ProSLIC to the W&G PCM-4”
- “AN55: Si3220/Si3225 User Guide”

Protection Circuitry

Figure 2 shows a surge protection circuit arrangement that supports a number of different population options. This is the same protection circuit that is featured in the Si3220DC0-EVB and Si3225DC0-EVB evaluation board designs (see Table 3).

The over-voltage protection aspect of the surge protection circuit must consider the most negative battery voltage that is used in the line card design and the maximum voltage that can be tolerated by the linefeed circuitry. The linefeed circuit can be the Si3200, which can safely tolerate up to 100 V, or a discrete bipolar transistor linefeed, which is typically capable of safely tolerating up to 200 V or even 300 V, depending on the voltage ratings of the selected discrete transistors.

For cases where the most negative battery voltage in the system is substantially less than the maximum voltage tolerated by the linefeed circuit, it is possible to use fixed-voltage clamping devices, such as D3 and D4, as shown in Figure 2 (in this case, U4 is not installed). In this case, the maximum clamping voltage for the clamping device must be less than the absolute value of the maximum voltage tolerated by the linefeed and greater than the absolute value of the most negative battery supply. This requirement is expressed in Equation 44.

$$V_{CLAMP(max)} < |V_{LF(max)}|$$
$$V_{CLAMP(min)} > |V_{BATH}|$$

Equation 44.Fixed Voltage Clamp Selection

where

- $V_{LF(max)}$ is the absolute maximum voltage rating of the linefeed (Si3200 or discrete)
- $V_{CLAMP(max)}$ is the maximum clamping voltage for the voltage clamping device
- $V_{CLAMP(min)}$ is the minimum clamping voltage for the voltage clamping device

In cases where the most negative battery voltage is near the maximum voltage safely tolerated by the linefeed circuit, it becomes necessary to use a battery tracking clamping device, such as U4, as shown in Figure 2 (in this case, D3 and D4 are not installed).

The overcurrent devices (RF1/RF2 or RF5/RF6 in Figure 2) must be selected taking into consideration the requirements of the application (e.g. Bellcore GR-1089, ITU-T K.20, K.21, UL60950/EN60950, etc.) with respect to the current-limiting device rated surge current waveform capabilities and ac power fault capabilities. The surge current waveform and ac power fault capabilities of the voltage-clamping device must also be considered with respect to the application’s requirements.

The following sub-sections provide the recommended component population options for the circuit, shown in Figure 2, which are applicable to various typical applications and surge requirements.

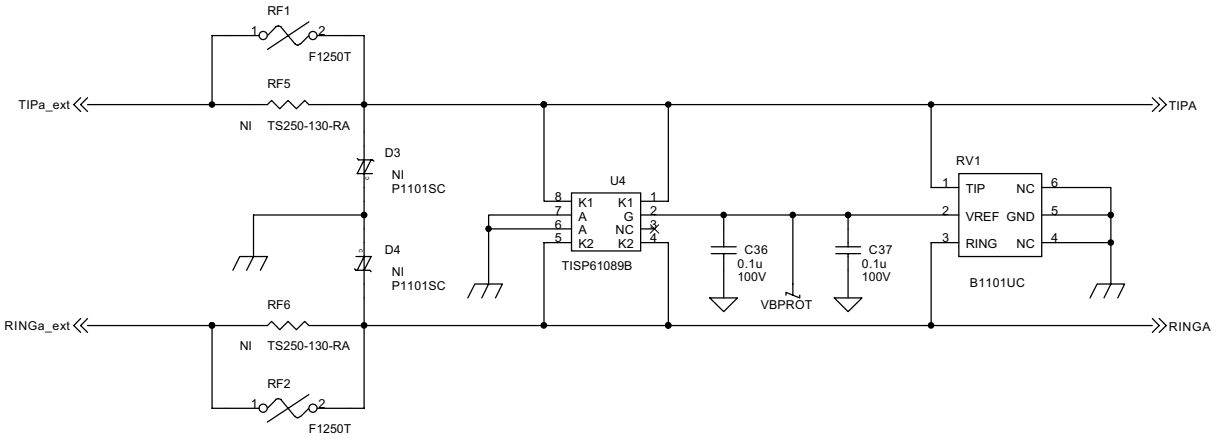

Figure 2. Surge Protection Circuitry

Si3220 with Discrete Linefeed (Int. Ringing, VBATH = –150 V)

The arrangement and components recommended in this section satisfy the lightning surge and ac power fault requirements set forth in Bellcore GR-1089, ITU-T K.20 and K.21.

When using a discrete bipolar transistor linefeed with internal ringing, the most negative battery voltage may be selected to be as much as –160 V. In this case, a most-negative battery tracking voltage-clamping arrangement is required. Follow the population options provided in Table 14.

Table 14. Discrete Linefeed (Internal Ringing, VBATH = -150V)

Reference Number	Recommended Manufacturer	Recommended Part Number	Comments
D3, D4	—	—	Not installed
U4	Bourns	TISP61089B	For battery voltages up to –155 V
RF1, RF2	—	—	Not installed
RF5, RF6	MMC or Bourns	L11A050AA 4B06B-522-RC	Thick film surge resistors

Si3225 with Si3200 Linefeed (External Ringing)

The arrangement and components recommended in this section satisfy the lightning surge and AC power fault requirements set forth in Bellcore GR-1089, ITU-T K.20 and K.21.

When the Si3225 is used in conjunction with an external ringing source, said ringing source is assumed to have its own protection circuitry (not shown in Figure 2). The Si3200 linefeed device is rated for a maximum voltage of 100 V. Thus, the determining factor for the selection of the over-voltage clamping device is the value of the most negative battery voltage in the system. If the most negative voltage in the system is close to the maximum rating of the Si3200 (i.e. –100 V), then follow the population scheme shown in Table 14. On the other hand, if the most negative battery voltage in the system is well above –100 V (e.g. –72 V), use a fixed clamping voltage device with a maximum clamping voltage that is less than 100 V and a minimum clamping voltage that is greater than the absolute value of the most negative battery voltage. Table 15 provides an example for V_{BATH} = –72 V.

Table 15. Si3200 Linefeed (Internal Ringing, VBATH = –72 V)

Reference Number	Recommended Manufacturer	Recommended Part Number	Comments
D3, D4	Teccor	P0901SC	V_{DRM} = 75 V, V_S = 98 V
U4	—	—	Not installed
RF1, RF2	—	—	Not installed
RF5, RF6	MMC or Bourns	L11A050AA 4B06B-522-RC	Thick film surge resistors.

PCB Design Guidelines

In order to realize high-quality, low-noise performance and to optimize thermal dissipation, it is extremely important to follow the PCB layout guidelines recommended by Silicon Laboratories.

Refer to AN55 “Si3220/Si3225 User Guide” where detailed layout recommendations are provided.

Excel Design Tool

This application note is provided with a companion Microsoft® Excel Workbook that allows the user to enter the design parameters of the application and computes the various equations presented in this document. This

Excel file plots the power dissipation of the Si3200 line feed device as a function of total loop resistance in the Fwd/Rev Active off-hook state. The Excel workbook also provides fast computation of supply currents and power consumptions for any arbitrary combination and number of channels in any of the possible states (i.e. SLEEP, OPEN, STANDBY, OHT, ACTIVE and RINGING).

This Excel tool is used in the next section to calculate the various parameter values associated with a design example.

Short Loop Design Example

Table 16 provides the parametric requirements of a typical short loop line card design, such as a VoIP application.

Table 16. Design Example #1 Parameters

Parameter Symbol	Value	Units	Comments
$T_{a.max}$	70*	^oC	Maximum ambient temperature
L_{max}	2000*	Feet	Maximum loop length in feet
r_w	0.09*	Ω/ft	AWG 24
$R_{LOOP.MAX}$	180	W	Maximum loop dc resistance
$R_{cpe.min}$	140*	W	Minimum CPE resistance
$R_{cpe.max}$	430*	W	Maximum CPE resistance
I_{LIM}	25*	mA	ILIM register setting
I_{BIAS}	4	mA	ABIAS register setting
maxREN	5*	unitless	Maximum ringer equivalence number
$V_{ring.CPE.min}$	40*	V_{rms}	Minimum CPE ringing voltage (RMS)
f_{RING}	20*	Hz	Nominal ring frequency
V_{OFF}	0*	Volts	Ringing dc offset (See “AN86: Ringing/Ringtrip Operation and Architecture on the Si3220/Si3225”)
V_{OVRING}	0*	Volts	Ringing overhead (typically 0 V)
V_{DD}	5*	Volts	Supply voltage
V_{CM}	3*	Volts	Typical VCM RAM setting
V_{OV}	4*	Volts	Typical VOVRAM setting
k	0.9*	unitless	Power dissipation margin factor
***Note:** These values are entered into the “Parameters” worksheet of the AN88 workbook.			

Si3220 vs. Si3225 Selection

Since the application is for a relatively short loop (2000 ft. max.), the ringing requirements can be supported with internal ringing and, therefore, the Si3220 is selected.

Temperature Grade Selection

The application calls for a 0 °C to +70 °C device temperature grade. The corresponding ordering part numbers are Si3200-KS and Si3220-KQ.

AN88 Workbook Computations

Table 17 shows the computations for this design example carried out by the companion Excel workbook.

The Excel workbook selects VBATL = –30 V and VBATH = –78. The user may manually enter other values for VBATL and VBATH in the “Power Dissipation Graph” worksheet.

Table 17. Short Loop Design Example Computations

AN88 Equation No.	Symbol	Value	Units	Comments
1	$P_{d.max.Si3200}$	1.273	W	Maximum allowable power dissipation for the Si3200
1	$P_{d.max.Si322x}$	2.800	W	Maximum allowable power dissipation for the Si322x
5	$\|VBATL_{min}\|$	17.8	V	Minimum low battery voltage (absolute value)
7	$\|VBATL_{max}\|$	42.5	V	Maximum low battery voltage (absolute value) (k = 0.9)
Selected	VBATL	–30	V	Selected VBATL (midpoint between $VBATL_{min}$ and $VBATL_{max}$)
8	$V_{ring.RMS.min}$	54.3	V(RMS)	Minimum required ringing voltage (RMS)
10	R_{SW}	920	Ohms	Battery switching point in terms of loop + CPE resistance
—	L_{SW}	5444	ft	Battery switching point in terms of loop length
9	$\|VBATH_{min}\|$	77.78	V	Minimum high battery voltage (absolute value)
11	$\|VBATH_{max}\|$	59.40	V	Maximum high battery voltage (absolute value)
Selected	$V_{ring.rms}$	55	V(RMS)	Selected ringing voltage (RMS)
Selected	VBATH	–78	V	Selected VBATH
18	V_{thres}	26.0	V	Battery switching threshold in terms of V_{RING} voltage
19	BATHTH	1534	Hexadecimal	Battery high threshold RAM value
20	BATLTH	1434	Hexadecimal	Battery low threshold RAM value
21	BATLPF	A0E	Hexadecimal	Battery switching LPF coefficient RAM value
Look-up	$I_{DD.SLEEP}$	1.110	mA	V_{DD} supply current per-channel in SLEEP mode.
Look-up	$I_{DD.OPEN}$	20.110	mA	V_{DD} supply current per-channel in OPEN mode.
Look-up	$I_{DD.STBY}$	20.110	mA	V_{DD} supply current in Fwd/Rev Active On-Hook STANDBY mode.

Table 17. Short Loop Design Example Computations (Continued)

Look-up	$I_{DD.OHT}$	60.110	mA	V_{DD} supply current per-channel On-Hook transmit mode (OHT)
22	$I_{DD.A}$	63.00	mA	V_{DD} supply current per-channel in ACTIVE mode
30	$I_{DD.R}$	54.8	mA	V_{DD} supply current per-channel in SINUSOIDAL RINGING mode
Look-up	$I_{VBAT.SLEEP}$	0.100	mA	V_{BAT} supply current per-channel in SLEEP mode.
Look-up	$I_{VBAT.OPEN}$	0.225	mA	V_{BAT} supply current per-channel in OPEN mode.
Look-up	$I_{VBAT.STBY}$	0.400	mA	V_{BAT} supply current per-channel in STANDBY mode.
Look-up	$I_{VBAT.OHT}$	8.400	mA	V_{BAT} supply current per-channel in On-Hook transmit mode (OHT).
23	$I_{VBAT.A}$	29.40	mA	V_{BAT} supply current per-channel in ACTIVE mode
31	$I_{VBAT.R}$	28.8	mA	V_{BAT} supply current per-channel in SINUSOIDAL RINGING mode
29	$I_{AVE.RING.SINE}$	28.8	mA	Average ringing current (sinusoidal, Rloop = 0)
25	$P_{Si3200.A\ @\ VBATL}$	0.779	W	Maximum Si3200 power dissipation in ACTIVE mode @ VBATL
26	$P_{Si3200.A\ @\ VBATH}$	0.824	W	Maximum Si3200 power dissipation in ACTIVE mode @ VBATH
27	$P_{Si322x.A}$	0.298	W	Si322x power dissipation in ACTIVE mode
32	$P_{Si3200.R}$	0.248	W	Si3200 power dissipation in SINUSOIDAL RINGING mode
33	$P_{Si3220.RING.SINE}$	0.254	W	Si322x power dissipation in SINUSOIDAL RINGING mode
Note: All supply currents and power dissipations are per-channel. All computations and looked-up values assume ABIAS and OBIAS are set to 4 mA (See AN88).				

Figure 3 shows the Si3200 power dissipation during Fwd/Rev Active Off-Hook as plotted by the AN88 Excel workbook.

The required 2000ft. maximum loop length plus off-hook CPE resistance (equivalent to 180 Ω + R_{cpe}) will be serviced entirely by VBATL from a dc feed standpoint, as seen in Figure 3, with ample power dissipation margin.

Meanwhile, the selected VBATH = –78 V and Vring.rms = 55 Vrms will guarantee 40 Vrms of ringing signal being delivered to the CPE over the longest possible loop and into a 5 REN ringer load.

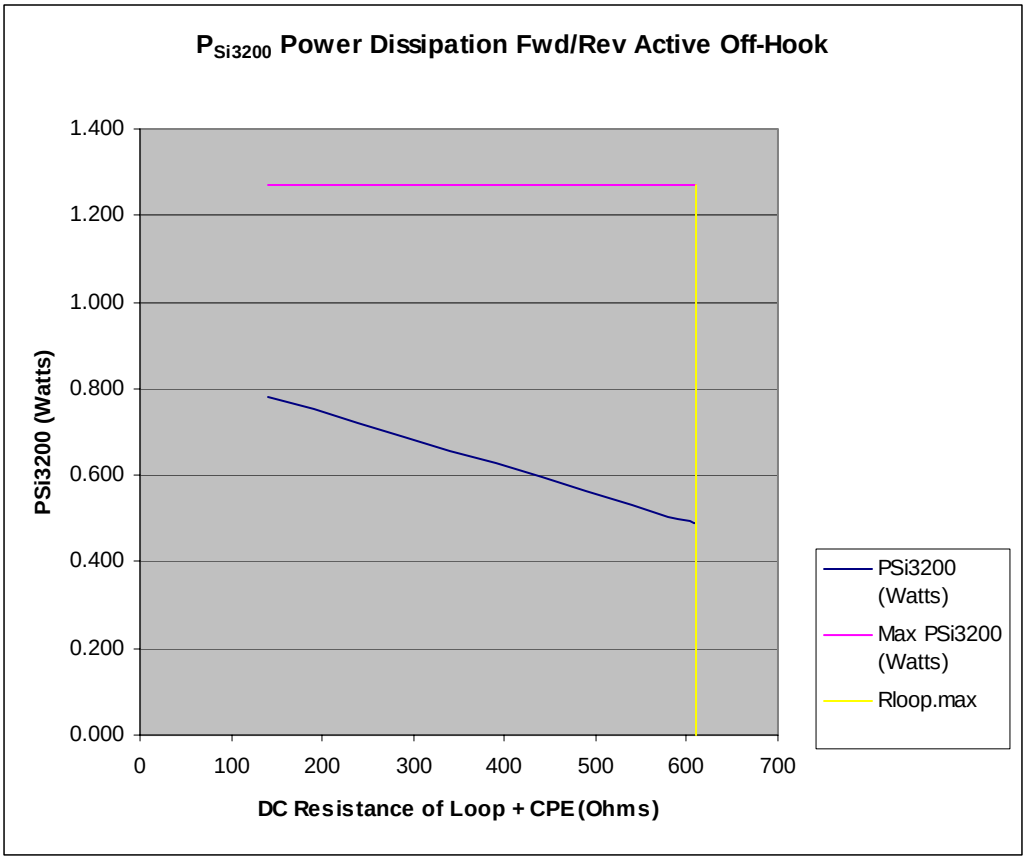

Figure 3. PSi3200 Power Dissipaton (@ VBATL and VBATH)

Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com